



MS-7302 VER:1.0

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD/ATI RS780 colay RS740

AMD/ATI SB700

On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111C(B)/RTL8101E

HD Codec -- ALC888

BIOS -- SPI ROM 8M

1394 -- JMB381

Main Memory:

DDR II X 2 (Max 4GB)

Expansion Slots:

PCI-E X 1 *1

PCI-E X 16 *1

PCI 2.2 Slot X 2

Clock Generator:

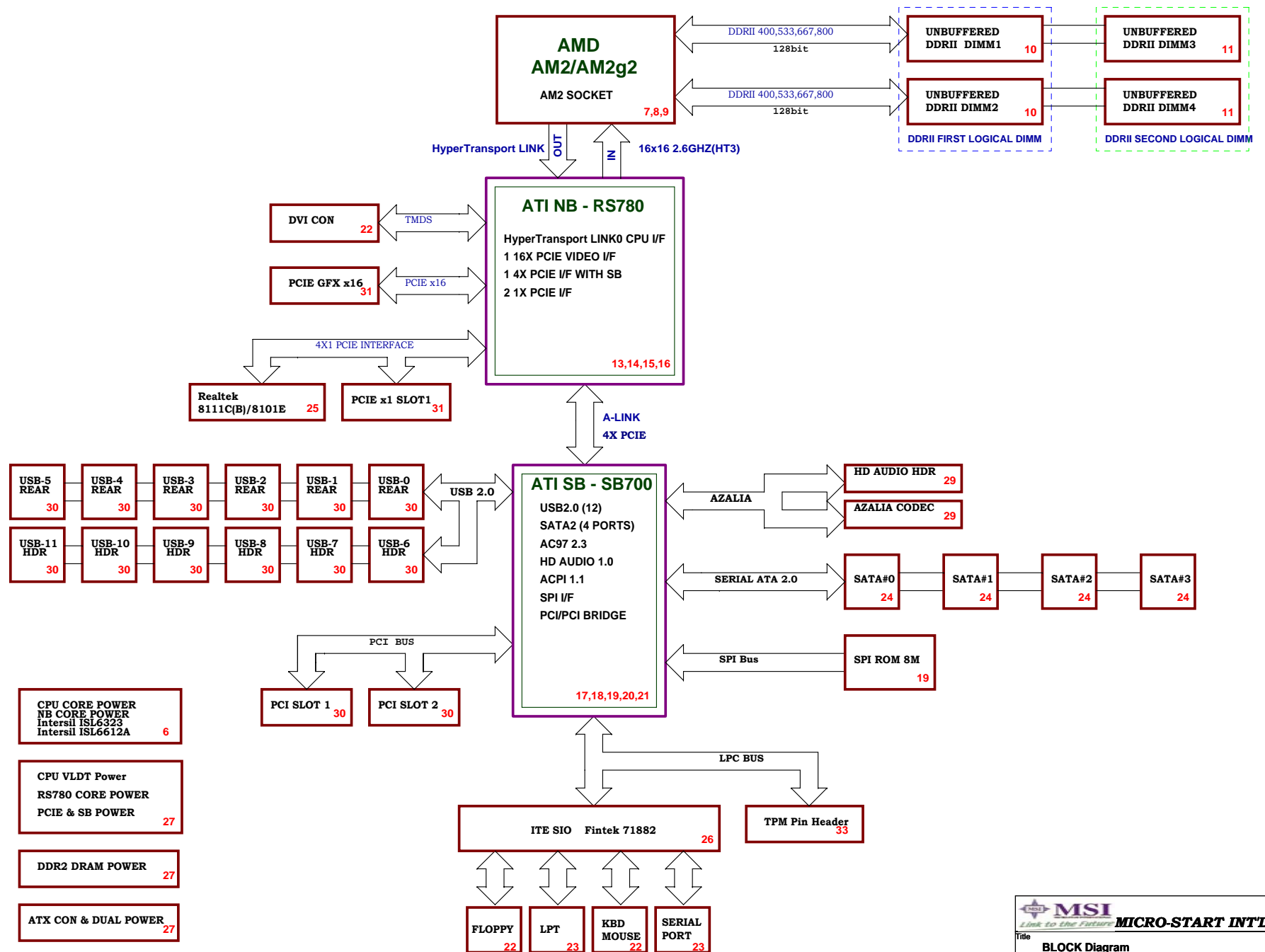
Controller--ICS9LPRS477

PWM:

INTSIL6566 3 Phase+75125

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Project RS-780 BLOCK DIAGRAM



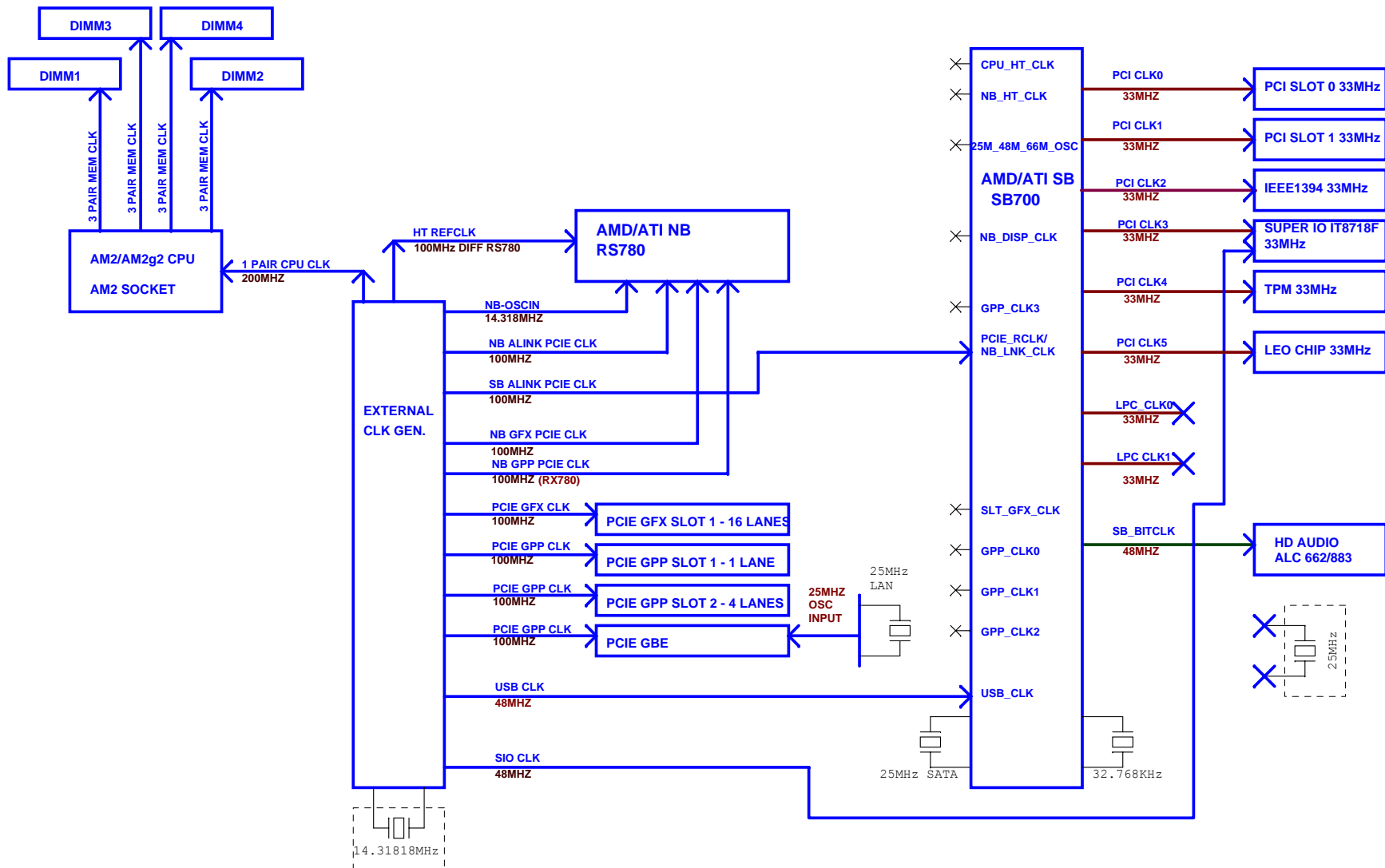
GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTEVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SM#/#EXTEVNT1#		LPC_SM#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

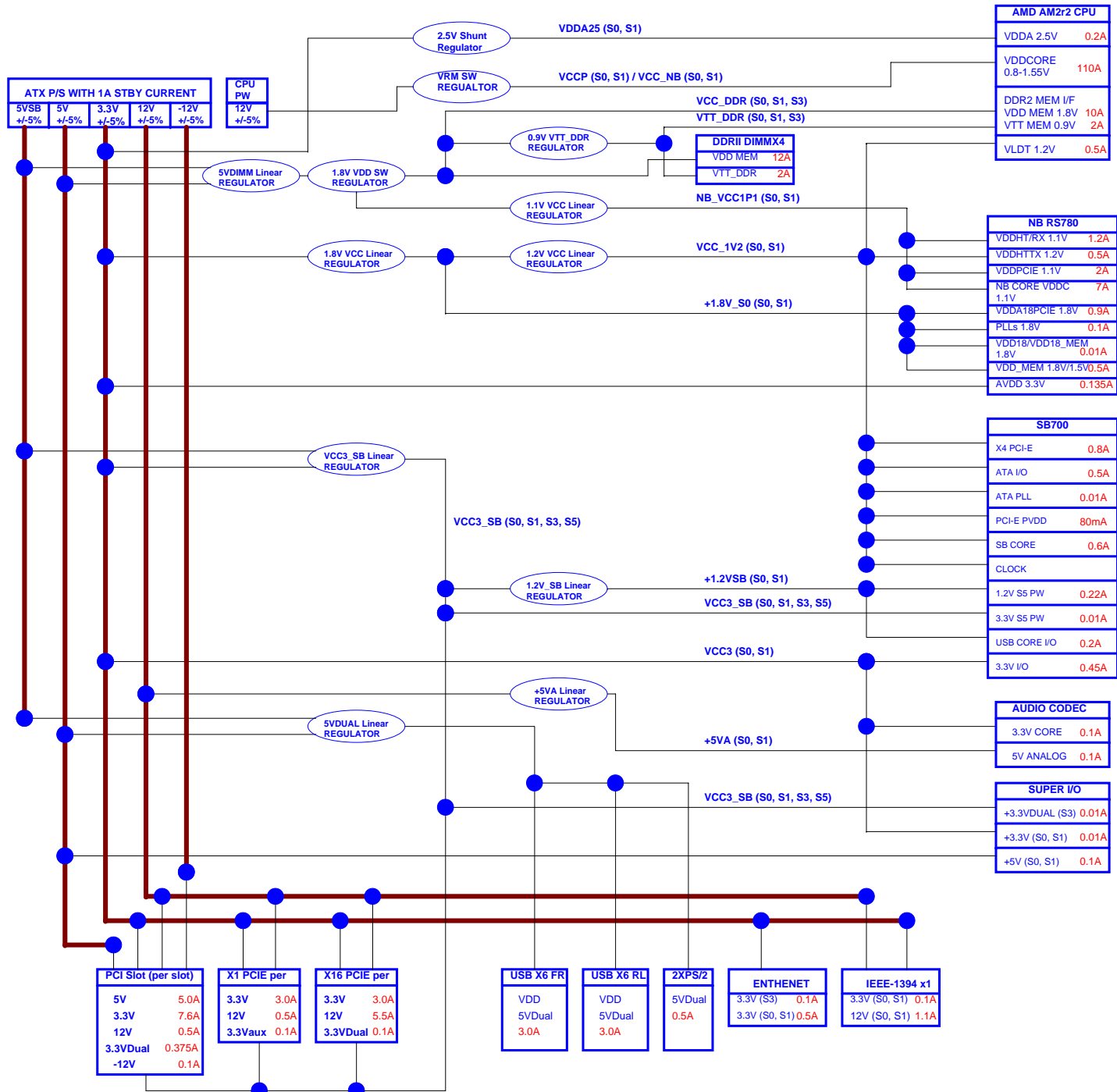
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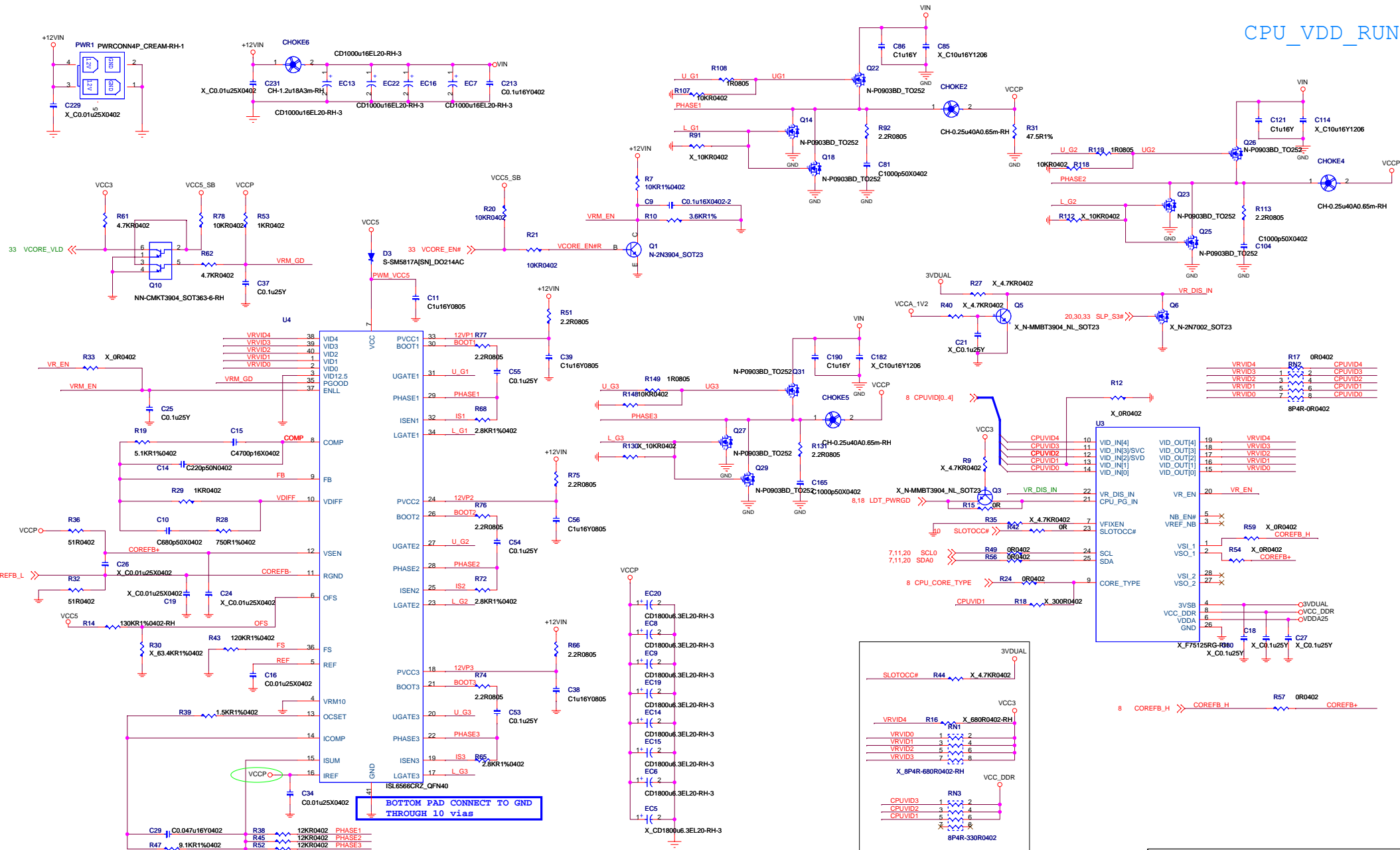
GPIO Name	Type	Function Description	Pin	Page
VIDO5/GP27		LEO_GPIO2	20	26
VIDO4/GP26		LEO_GPIO1	21	26
VIDO1/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SM#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SS_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

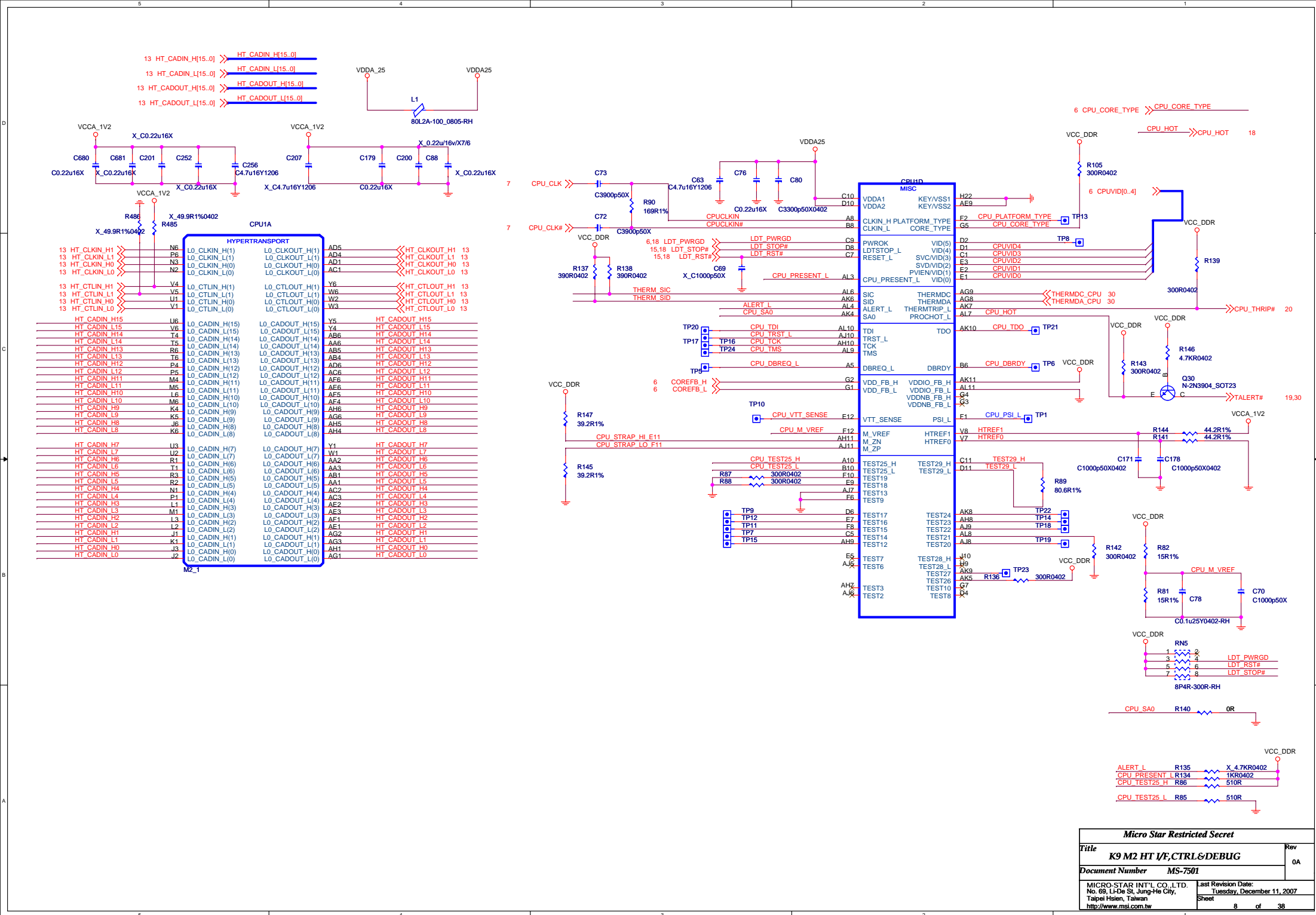
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD#	REQ#0 PGNT#0	AD16	PCICLK0
PCI Slot 2	PCI_INTB# PCI_INTC# PCI_INTD# PCI_INTA#	REQ#1 PGNT#1	AD17	PCICLK1



Power Deliver Chart







11 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
11 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
11 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
11,12 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
11 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

CPU1B

MEMORY INTERFACE A

11,12 MEM_MA0_CLK_H2 >> MEM_MA0_CLK_H2 AG21
11,12 MEM_MA0_CLK_L2 >> MEM_MA0_CLK_L2 AG20
11,12 MEM_MA0_CLK_H1 >> MEM_MA0_CLK_H1 G12
11,12 MEM_MA0_CLK_L1 >> MEM_MA0_CLK_L1 H19
11,12 MEM_MA0_CLK_H0 >> MEM_MA0_CLK_H0 U27
11,12 MEM_MA0_CLK_L0 >> MEM_MA0_CLK_L0 U26
11,12 MEM_MA0_CS_L1 >> MEM_MA0_CS_L1 AC25
11,12 MEM_MA0_CS_L0 >> MEM_MA0_CS_L0 AA24
11,12 MEM_MA0_ODT0 >> MEM_MA0_ODT0 AC28
AE20 MA1_CLK_H(2)
AE19 MA1_CLK_L(2)
G20 MA1_CLK_H(1)
G19 MA1_CLK_L(1)
V22 MA1_CLK_H(0)
W22 MA1_CLK_L(0)
AD23 MA1_CS_L(1)
AA23 MA1_CS_L(0)
AC23 MA1_ODT(0)
11,12 MEM_MA_CAS_L >> MEM_MA_CAS_L AB25
11,12 MEM_MA_WE_L >> MEM_MA_WE_L AB27
11,12 MEM_MA_RAS_L >> MEM_MA_RAS_L AA26
11,12 MEM_MA_BANK2 >> MEM_MA_BANK2 N25
11,12 MEM_MA_BANK1 >> MEM_MA_BANK1 Y27
11,12 MEM_MA_BANK0 >> MEM_MA_BANK0 AA27
12 MEM_MA_CKE1 >> MEM_MA_CKE1 L27
11,12 MEM_MA_CKE0 >> MEM_MA_CKE0 M25
MEM_MA_ADD15 M27
MEM_MA_ADD14 N24
MEM_MA_ADD13 N26
MEM_MA_ADD12 N26
MEM_MA_ADD11 P25
MEM_MA_ADD10 Y25
MEM_MA_ADD9 N27
MEM_MA_ADD8 R24
MEM_MA_ADD7 P27
MEM_MA_ADD6 R25
MEM_MA_ADD5 R26
MEM_MA_ADD4 T25
MEM_MA_ADD3 U25
MEM_MA_ADD2 T27
MEM_MA_ADD1 W24
MEM_MA_ADD0 MA_ADD(0)
MEM_MA_DQS_H7 AD15
MEM_MA_DQS_L7 AE15
MEM_MA_DQS_H6 AG18
MEM_MA_DQS_L6 AG19
MEM_MA_DQS_H5 AG24
MEM_MA_DQS_L5 AG25
MEM_MA_DQS_H4 AG27
MEM_MA_DQS_L4 AG28
MEM_MA_DQS_H3 D29
MEM_MA_DQS_L3 C29
MEM_MA_DQS_H2 C25
MEM_MA_DQS_L2 D25
MEM_MA_DQS_H1 F19
MEM_MA_DQS_L1 F19
MEM_MA_DQS_H0 F15
MEM_MA_DQS_L0 G15
MEM_MA_DM7 AE15
MEM_MA_DM6 AF19
MEM_MA_DM5 AJ25
MEM_MA_DM4 AH28
MEM_MA_DM3 B23
MEM_MA_DM2 E24
MEM_MA_DM1 F18
MEM_MA_DM0 H15
MA_DATA(63)
MA_DATA(62)
MA_DATA(61)
MA_DATA(60)
MA_DATA(59)
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MA_DATA(57)
MA_DATA(56)
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MA_DATA(34)
MA_DATA(33)
MA_DATA(32)
MA_DATA(31)
MA_DATA(30)
MA_DATA(29)
MA_DATA(28)
C27 MEM_MA_DATA27
G26 MEM_MA_DATA28
F27 MEM_MA_DATA29
C28 MEM_MA_DATA25
E27 MEM_MA_DATA26
F25 MEM_MA_DATA23
E25 MEM_MA_DATA22
E23 MEM_MA_DATA21
D23 MEM_MA_DATA20
E26 MEM_MA_DATA19
C26 MEM_MA_DATA18
G23 MEM_MA_DATA17
F23 MEM_MA_DATA16
E22 MEM_MA_DATA15
E21 MEM_MA_DATA14
F17 MEM_MA_DATA13
G17 MEM_MA_DATA12
G22 MEM_MA_DATA11
F21 MEM_MA_DATA10
G18 MEM_MA_DATA9
E17 MEM_MA_DATA8
G16 MEM_MA_DATA7
E15 MEM_MA_DATA6
G13 MEM_MA_DATA5
H13 MEM_MA_DATA4
H17 MEM_MA_DATA3
E16 MEM_MA_DATA2
E14 MEM_MA_DATA1
G14 MEM_MA_DATA0
MA_DQS_H(8)
MA_DQS_L(8)
MA_DM(8)
MA_CHECK(7)
MA_CHECK(6)
MA_CHECK(5)
MA_CHECK(4)
MA_CHECK(3)
MA_CHECK(2)
MA_CHECK(1)
MA_DM(0)
MA_CHECK(0)

11 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
11 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
11 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
11,12 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
11 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]

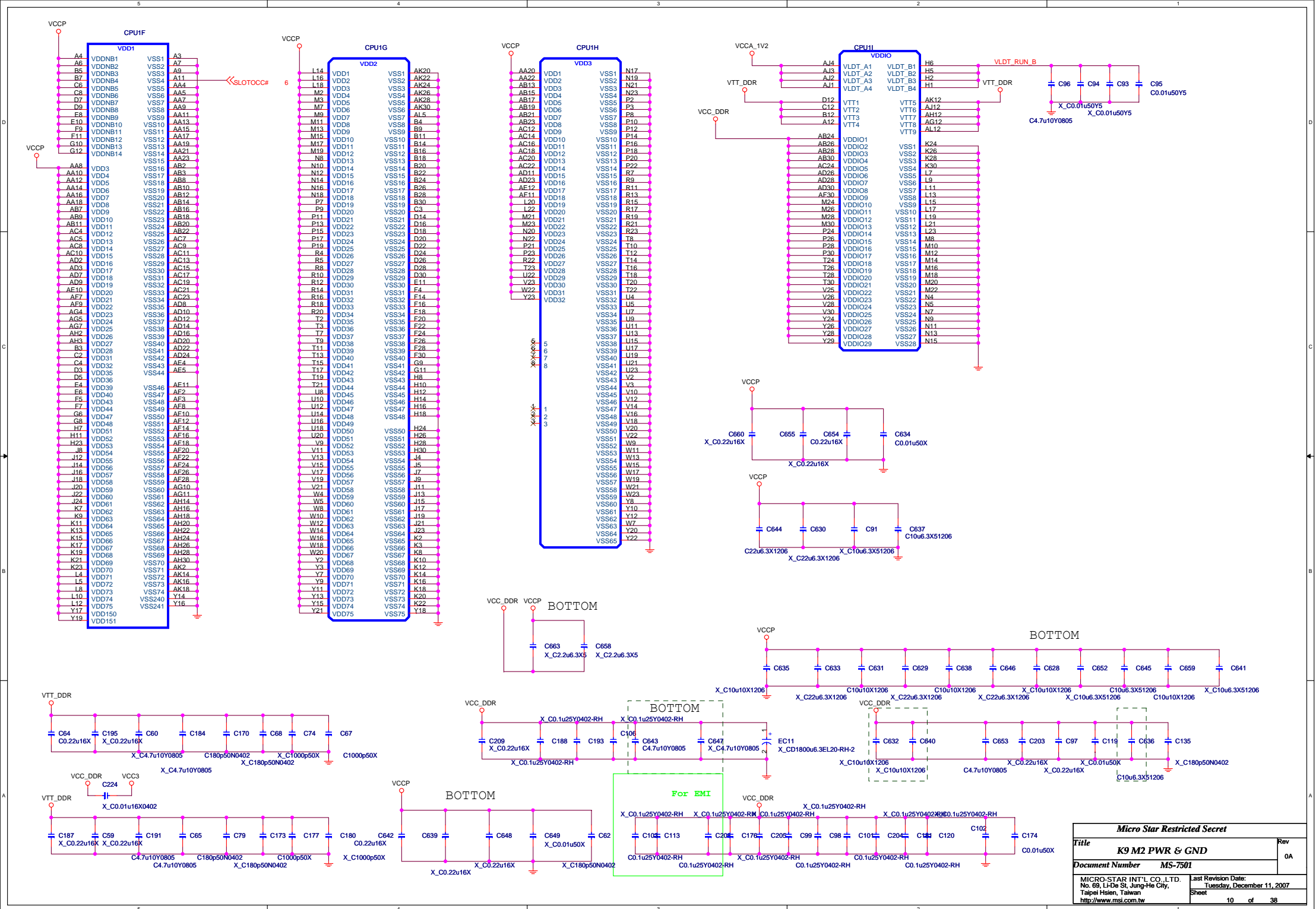
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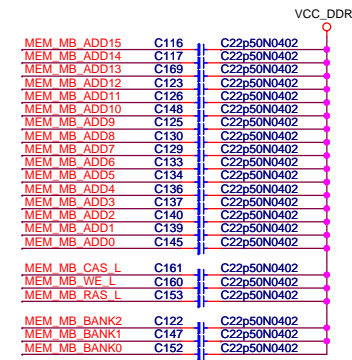
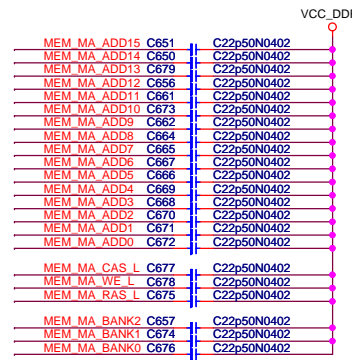
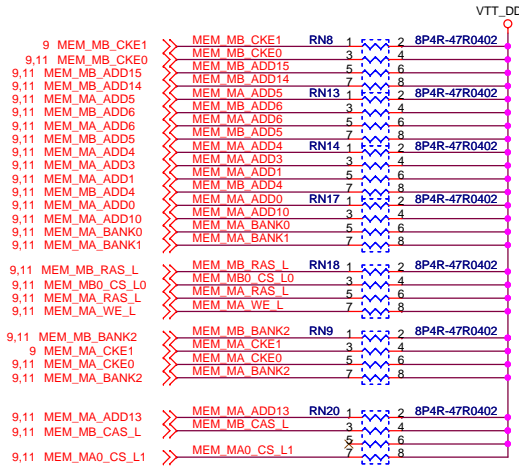
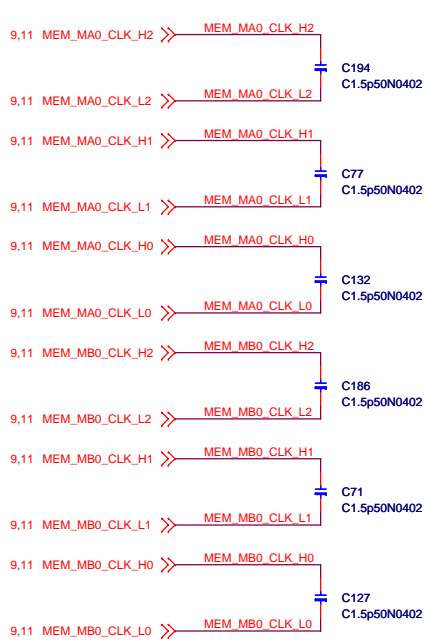
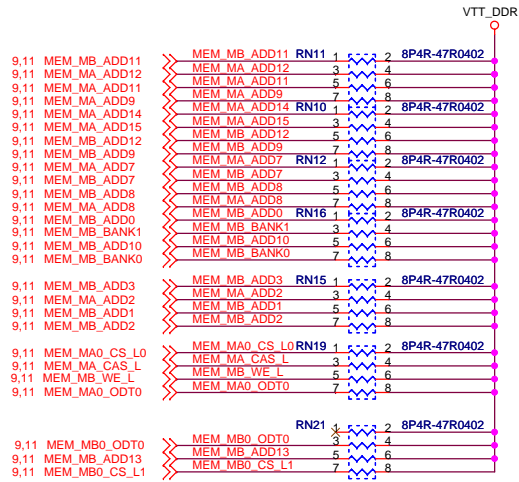
MEMORY INTERFACE B

11,12 MEM_MB0_CLK_H2 >> MEM_MB0_CLK_H2 AJ19
11,12 MEM_MB0_CLK_L2 >> MEM_MB0_CLK_L2 AK19
11,12 MEM_MB0_CLK_H1 >> MEM_MB0_CLK_H1 A18
11,12 MEM_MB0_CLK_L1 >> MEM_MB0_CLK_L1 A19
11,12 MEM_MB0_CLK_H0 >> MEM_MB0_CLK_H0 U31
11,12 MEM_MB0_CLK_L0 >> MEM_MB0_CLK_L0 U30
11,12 MEM_MB0_CS_L1 >> MEM_MB0_CS_L1 AE30
11,12 MEM_MB0_CS_L0 >> MEM_MB0_CS_L0 AC31
11,12 MEM_MB0_ODT0 >> MEM_MB0_ODT0 AD29
MB0_CLK_H(2)
MB0_CLK_L(2)
MB0_CLK_H(1)
MB0_CLK_L(1)
MB0_CLK_H(0)
MB0_CLK_L(0)
MB0_CS_L(1)
MB0_CS_L(0)
MB0_ODT(0)
MB1_CLK_H(2)
MB1_CLK_L(2)
MB1_CLK_H(1)
MB1_CLK_L(1)
MB1_CLK_H(0)
MB1_CLK_L(0)
MB1_CS_L(1)
MB1_CS_L(0)
MB1_ODT(0)
MB_CAS_L
MB_WE_L
MB_RAS_L
MB_BANK(2)
MB_BANK(1)
MB_BANK(0)
MB_CKE(1)
MB_CKE(0)
MEM_MB_ADD15 N28
MEM_MB_ADD14 N29
MEM_MB_ADD13 AE31
MEM_MB_ADD12 N30
MEM_MB_ADD11 P29
MEM_MB_ADD10 AA29
MEM_MB_ADD9 P31
MEM_MB_ADD8 R29
MEM_MB_ADD7 R28
MEM_MB_ADD6 R31
MEM_MB_ADD5 R30
MEM_MB_ADD4 T31
MEM_MB_ADD3 T29
MEM_MB_ADD2 U29
MEM_MB_ADD1 U28
MEM_MB_ADD0 AA30
MEM_MB_DQS_H7 AK13
MEM_MB_DQS_L7 AJ13
MEM_MB_DQS_H6 AK17
MEM_MB_DQS_L6 AJ17
MEM_MB_DQS_H5 AK23
MEM_MB_DQS_L5 AL23
MEM_MB_DQS_H4 AL28
MEM_MB_DQS_L4 AL29
MEM_MB_DQS_H3 D31
MEM_MB_DQS_L3 C31
MEM_MB_DQS_H2 C24
MEM_MB_DQS_L2 C24
MEM_MB_DQS_H1 D17
MEM_MB_DQS_L1 C17
MEM_MB_DQS_H0 C14
MEM_MB_DQS_L0 C13
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MB_DATA(5)
MB_DATA(4)
MB_DATA(3)
MB_DATA(2)
MB_DATA(1)
MB_DATA(0)
MB_DQS_H(8)
MB_DQS_L(8)
MB_DM(8)
MB_CHECK(7)
MB_CHECK(6)
MB_CHECK(5)
MB_CHECK(4)
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MB_CHECK(1)
MB_CHECK(0)

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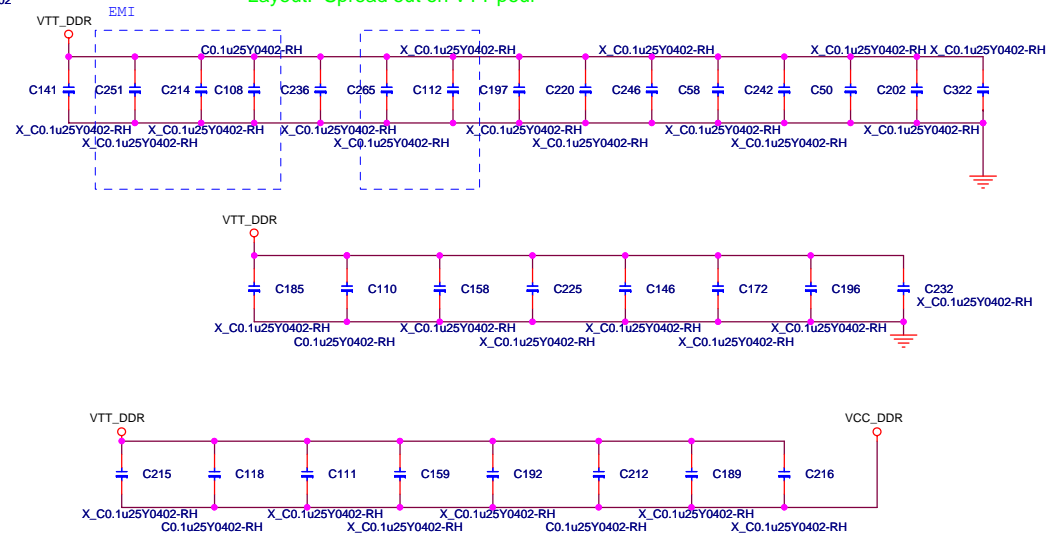
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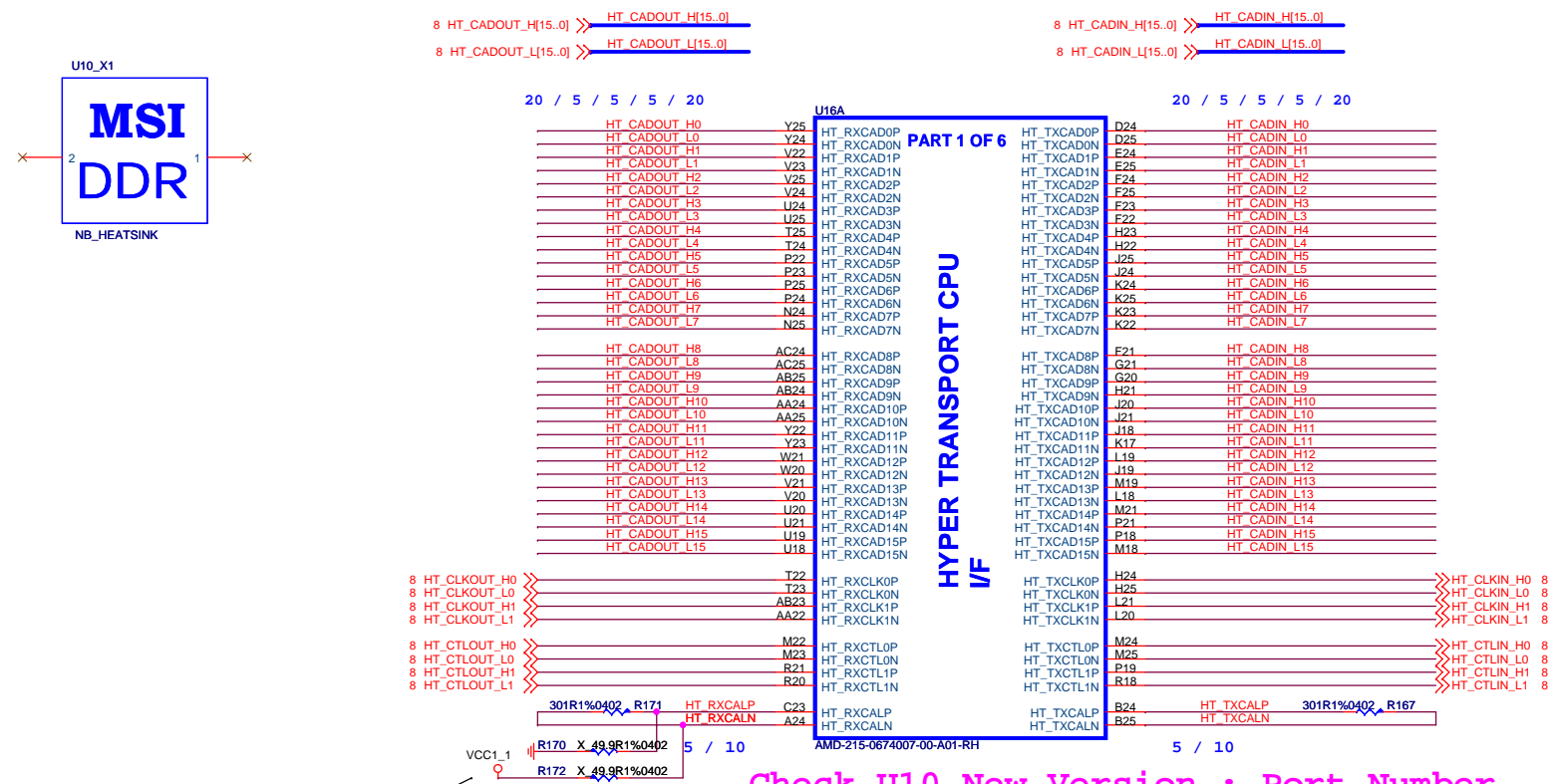


Decoupling Between Processor and DIMMs

Layout: Spread out on VTT pour



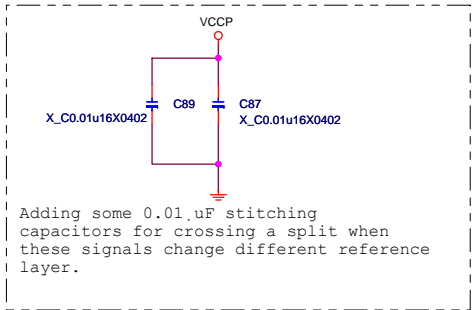
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MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, December 11, 2007 Sheet 12 of 38

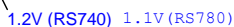


Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			

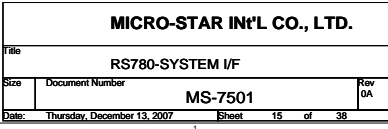


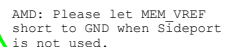
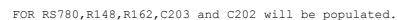


	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5





RS740/RX780/RS780: LOAD EEPROM STRAPS

15 RS740 DFT GPIO1 >> R243 150R0402



15 RS740 DFT GPIO0 >> R251 X_3KR0402



RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```

selects Loading of STRAPS from EPROM

```

```
RS780: pin SUS STAT#
```

Enables the Test Debug Bus using GPIO and/or memory IO

```
RS780: pin VSYNC
```

1. Disable (RS740/RS780)

1. Disable (RS740/RS780)

```
0 : Enable (RS740/RS780)
RS740: pin DET_GPIO0
```

```
RS740:  pin DFT_G
RS780:  pin HSYNC
```

AS780. PHH AS INC

Enables Test debug bus

using PCIE bus

1. Disable (can be enabled thru phofx register)

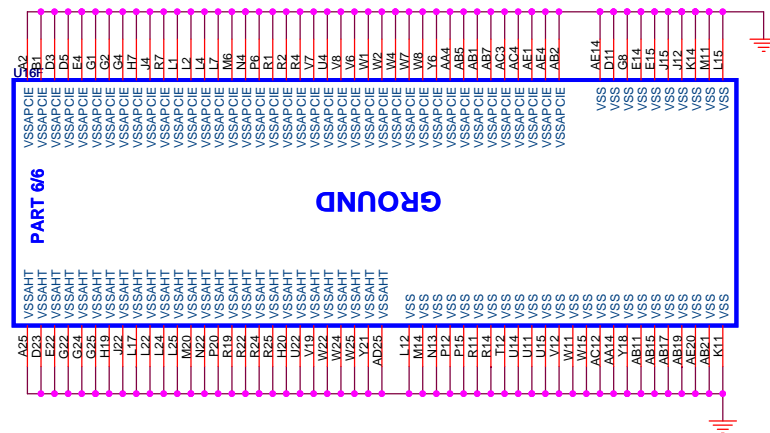
```
thru nbcfg register)
0 : Enable
```

0 : Enable

RS780: configurable thru register

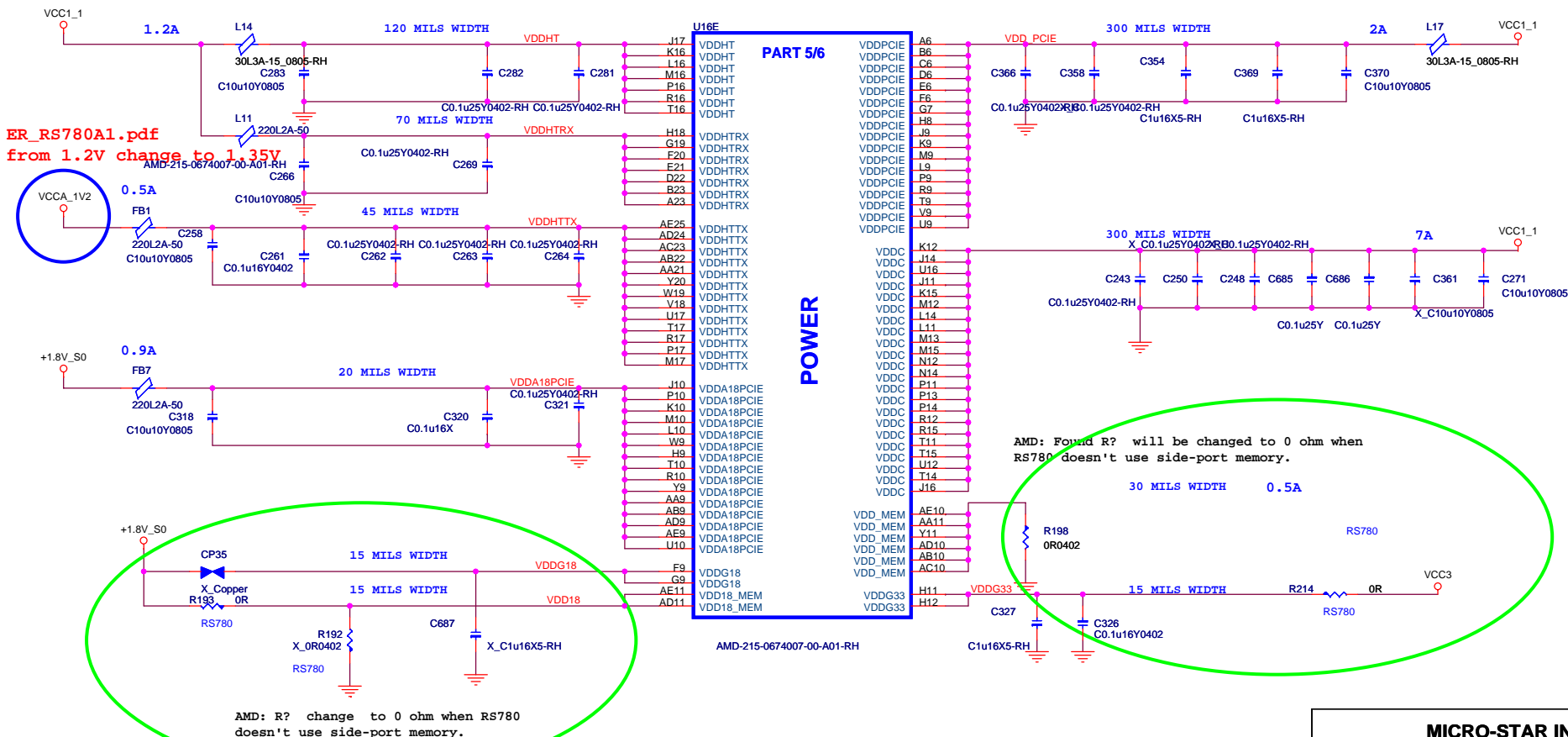
setting only

RS740: Not supported



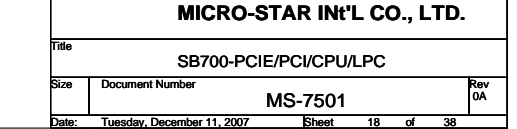
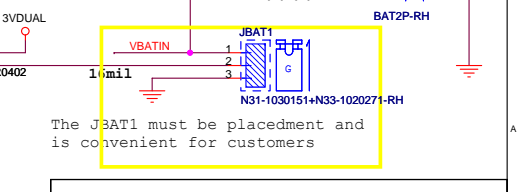
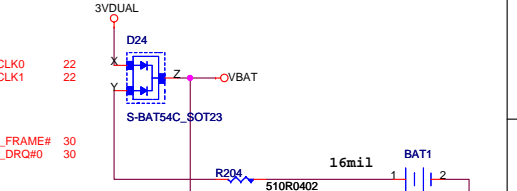
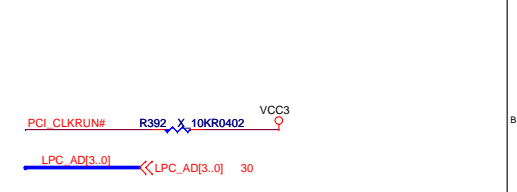
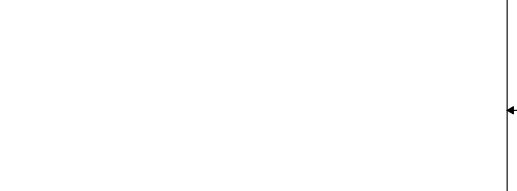
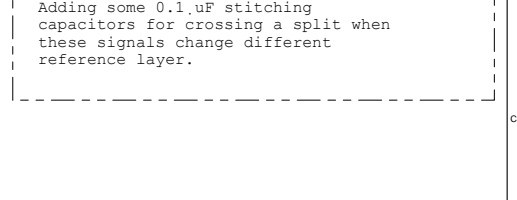
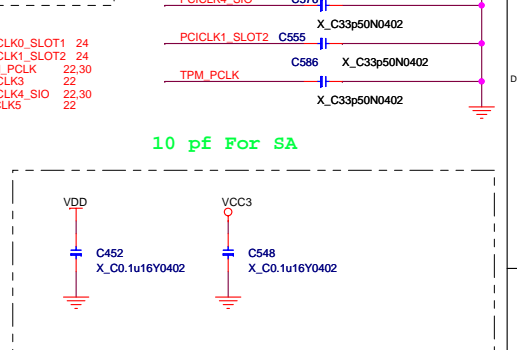
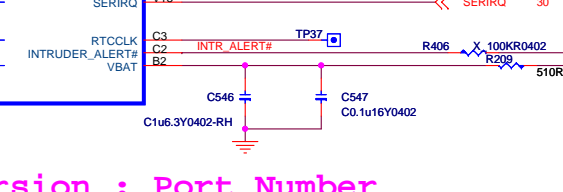
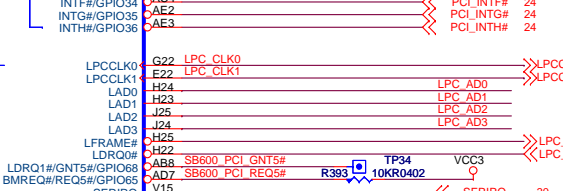
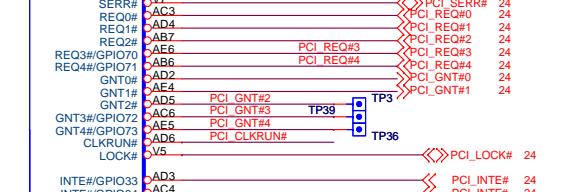
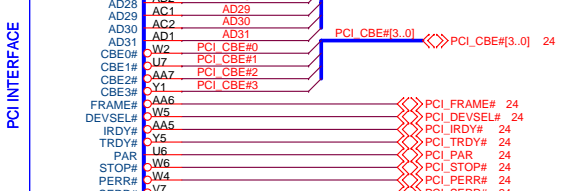
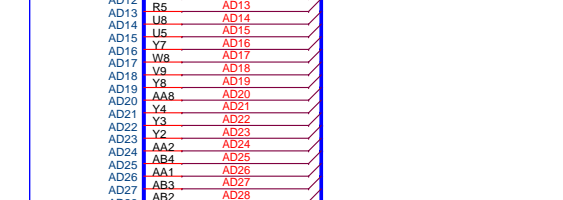
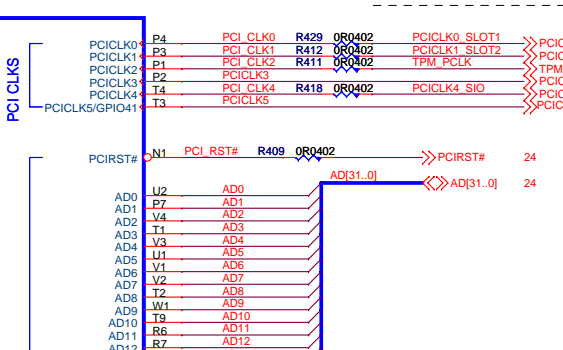
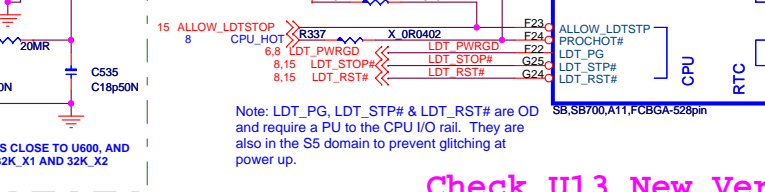
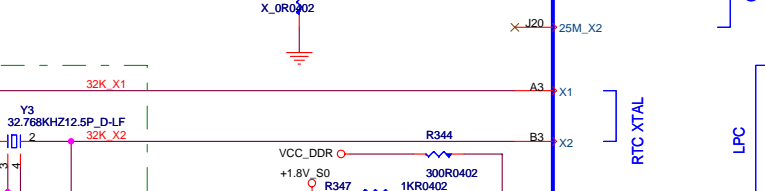
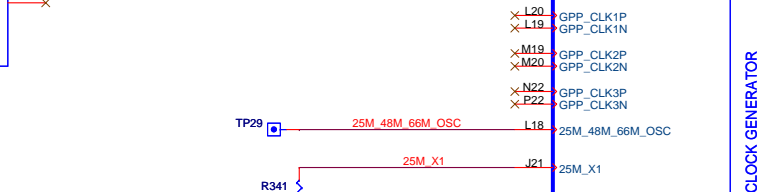
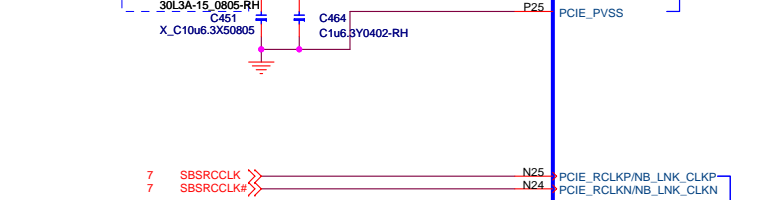
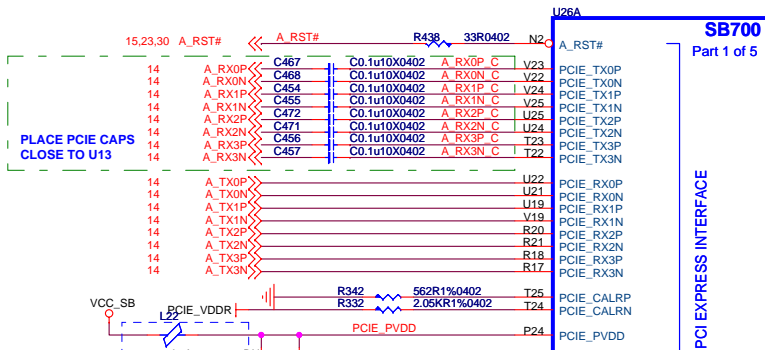
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC



MICRO-STAR IN'L CO., LTD.

Title			RS780-POWER	
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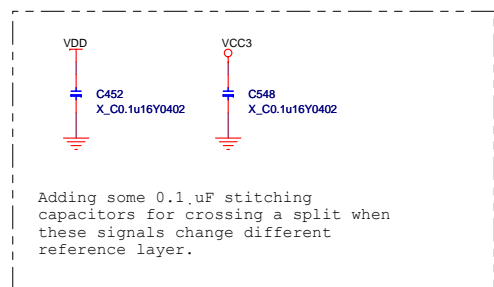


SIO PCICLK has been changed
PCICLK5 to PCICLK4 for AMD
recommand

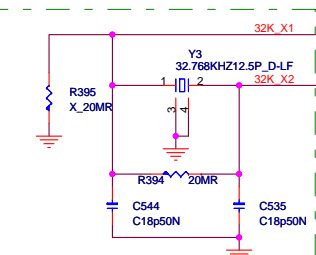
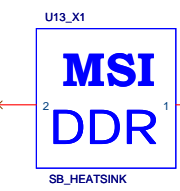
For EMI



10 pf For SA



SB HEAT-SINK



PLACE THESE COMPONENTS CLOSE TO U600, AND
USE GROUND GUARD FOR 32K_X1 AND 32K_X2

Note: LDT_PG, LDT_STP# & LDT_RST# are OD
and require a PU to the CPU I/O rail. They are
also in the S5 domain to prevent glitching at
power up.

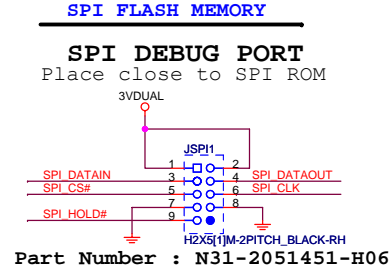
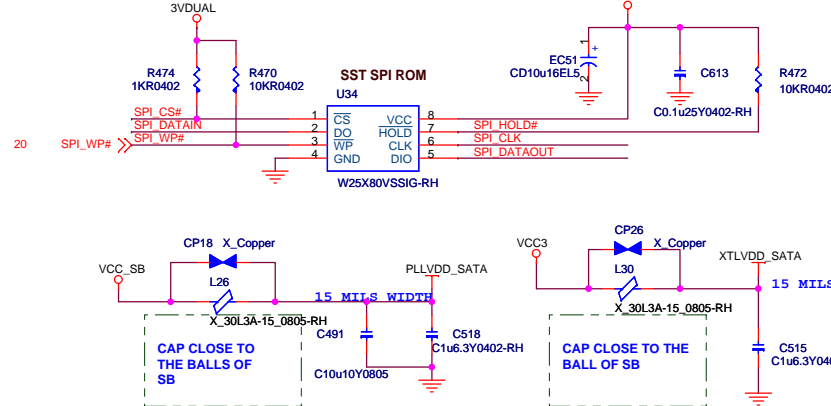
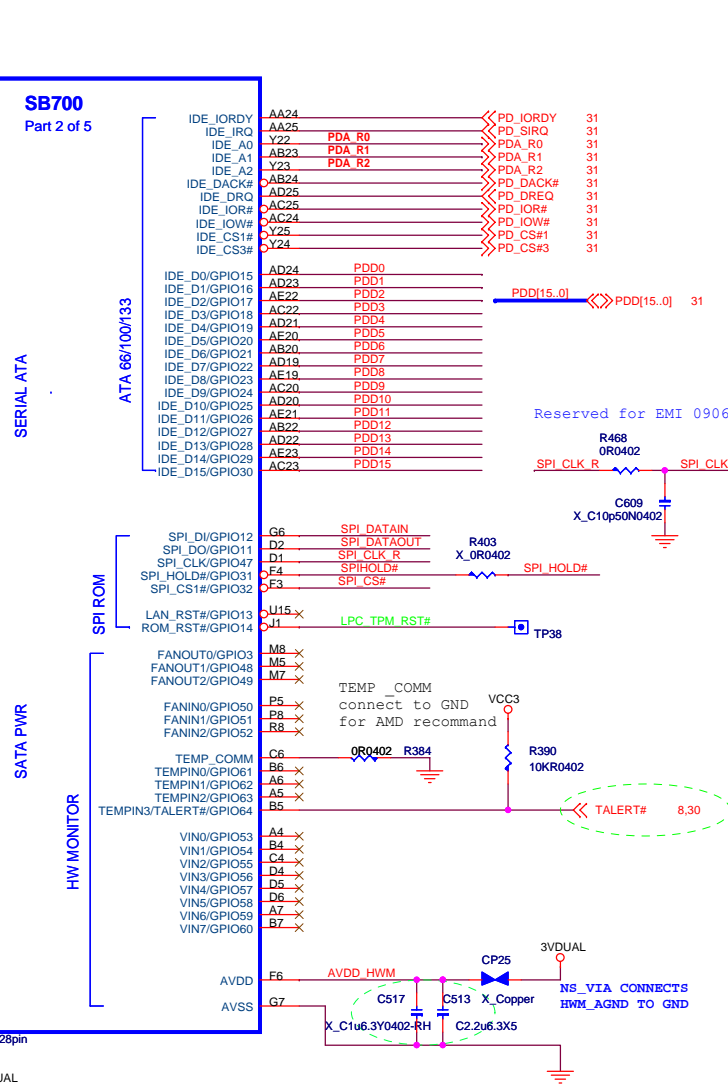
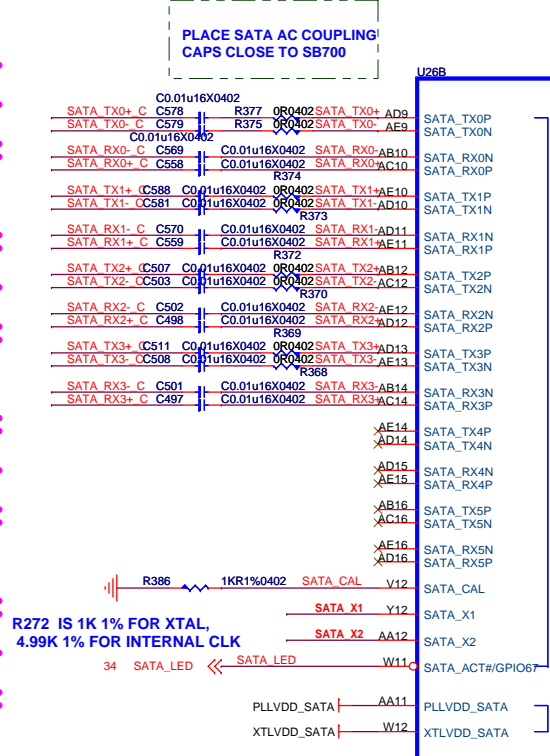
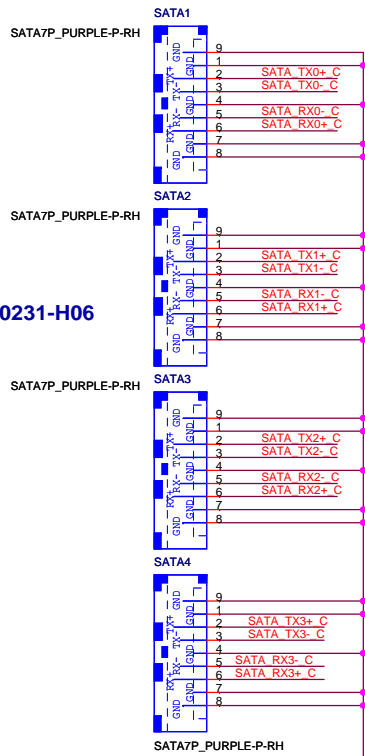
Check U13 New Version : Port Number

MICRO-STAR INT'L CO., LTD.			
Title SB700-PCIE/PCI/CPU/LPC			
Size	Document Number MS-7501		Rev 0A
Date:	Tuesday, December 11, 2007	Sheet	18 of 38

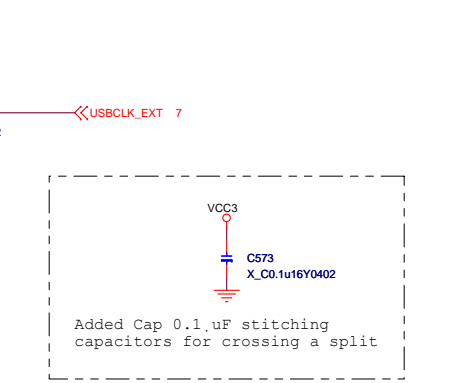
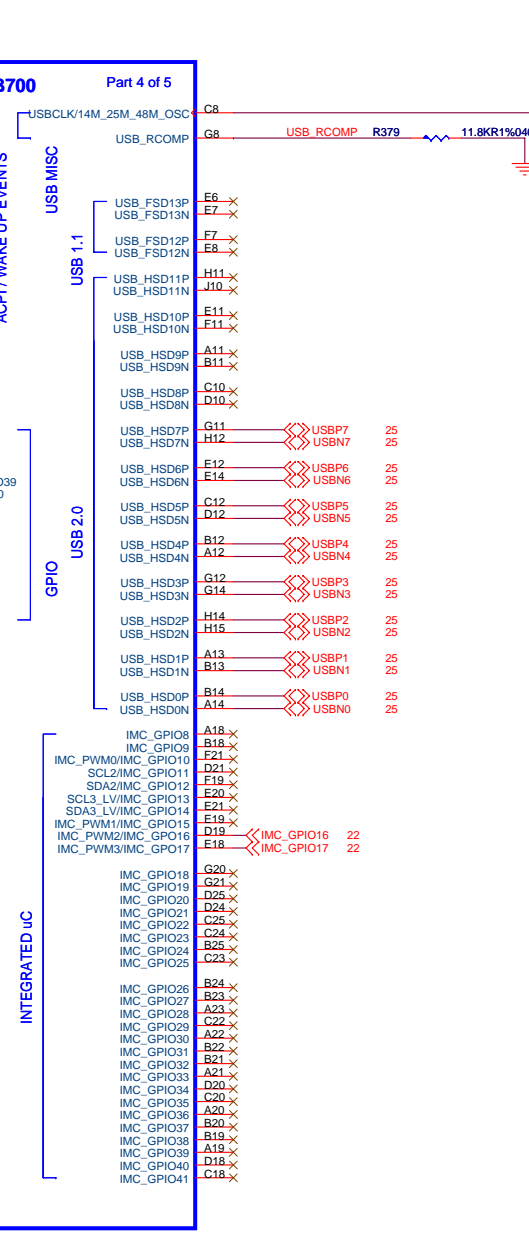
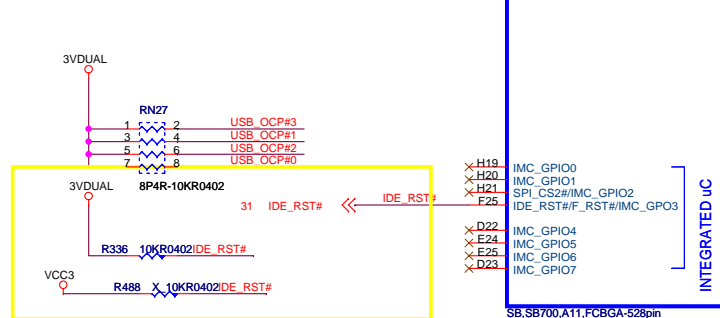
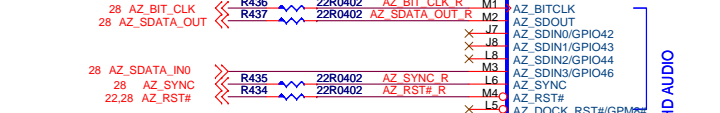
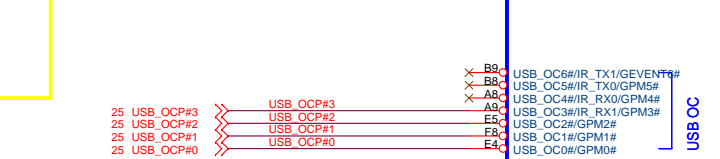
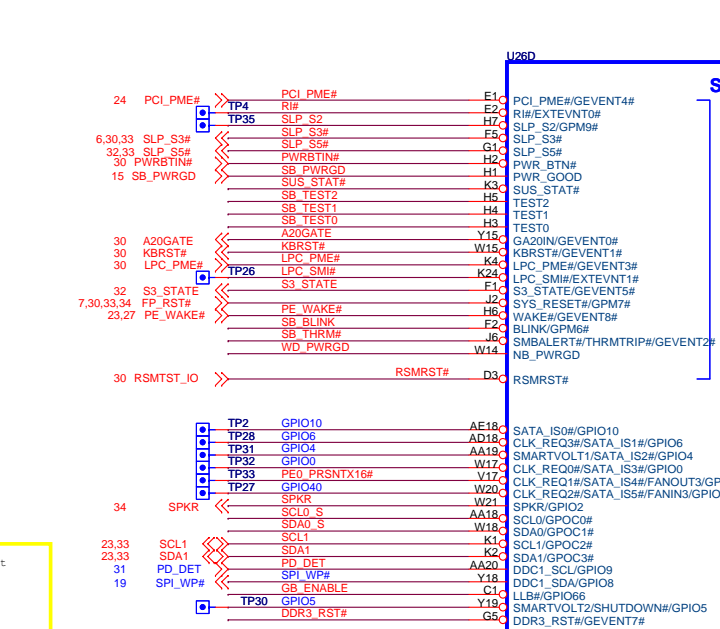
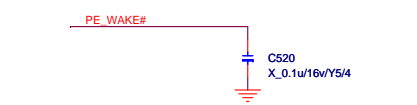
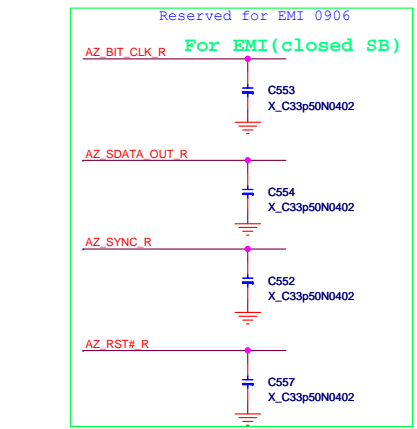
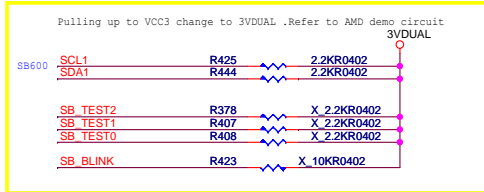
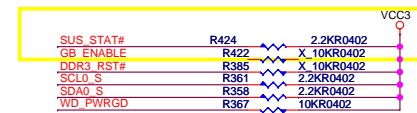
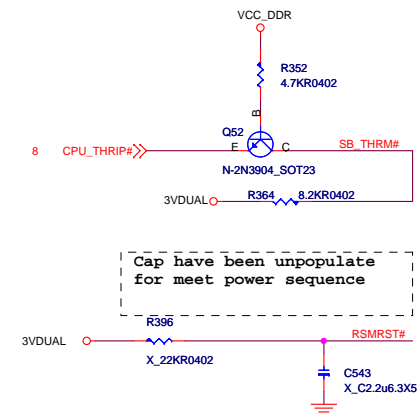


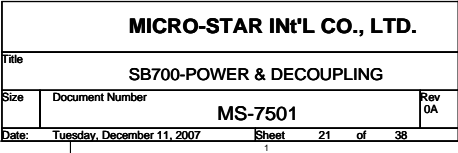
4 Ss	3 Ps
1 Pm	2 Sm

N5N-07M0231-H06



MICRO-STAR INT'L CO., LTD.			
Title SB700-SATA/IDE/HWM/SPI			
Size	Document Number	Rev 0A	
MS-7501			
Date:	Tuesday, December 11, 2007	Sheet	19 of 38

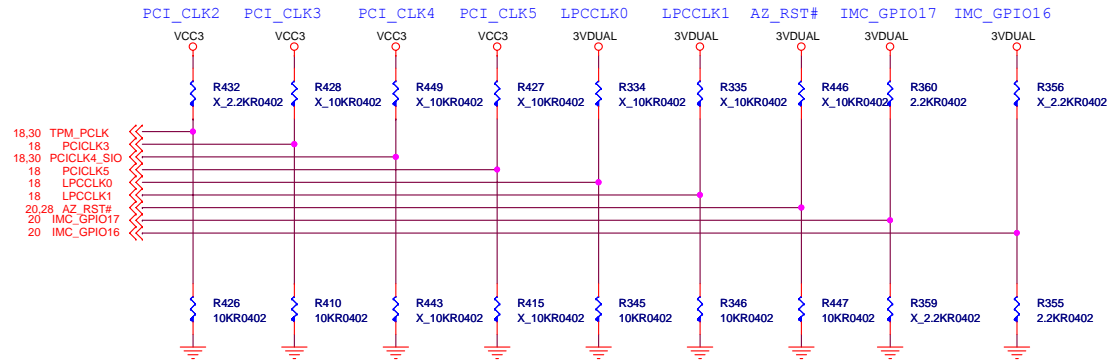






REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

MICRO-STAR INT'L CO., LTD.

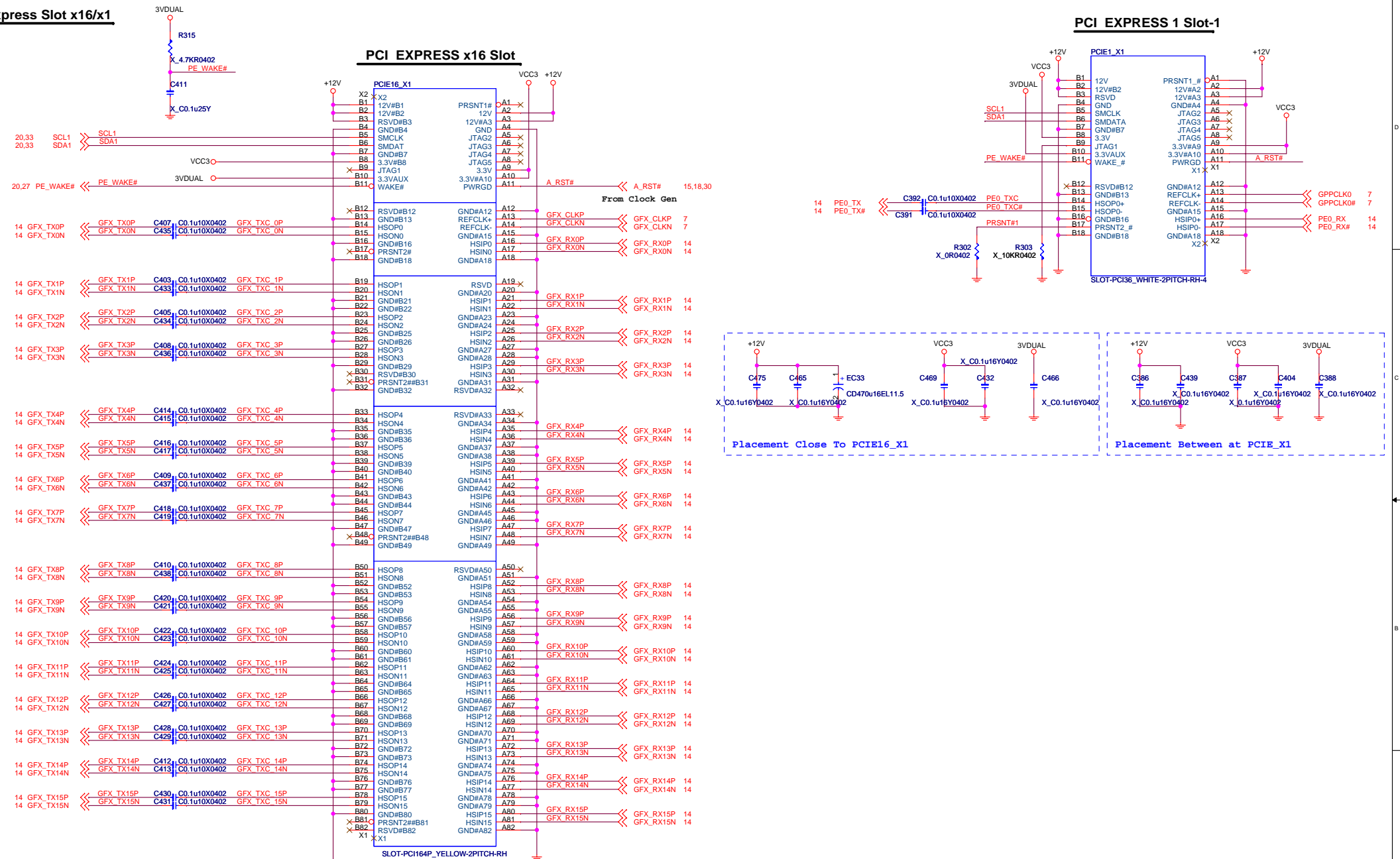
Title				SB700-STRAPS			
Size	Document Number						Rev 0A
MS-7501							
Date: Tuesday, December 11, 2007				Sheet	22	of	38

PCI Express Slot x16/x1

PCI EXPRESS 1 Slot-1

PCI EXPRESS x16 Slot

PCI1 X1



MICRO-START INT'L CO.,LTD.

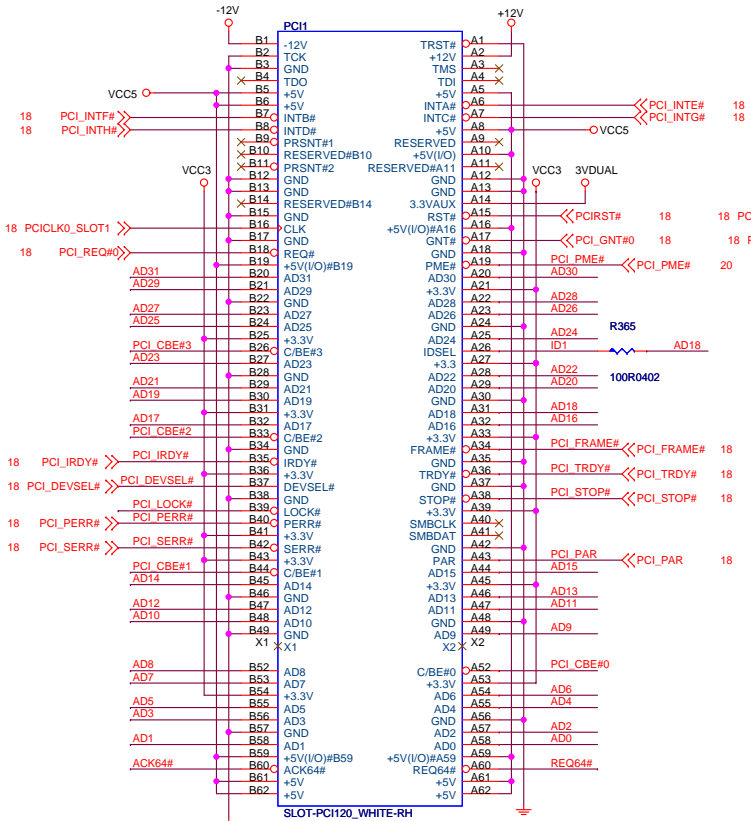
PCI EXPRESS X16 & X1 SLOT

Size	Document Number	Rev
Custom	MS-7501	0A

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 Sheet: 23 of 38

18 AD[31..0] >> AD[31..0]
18 PCI_CBE#[3..0] >> PCI_CBE#[3..0]

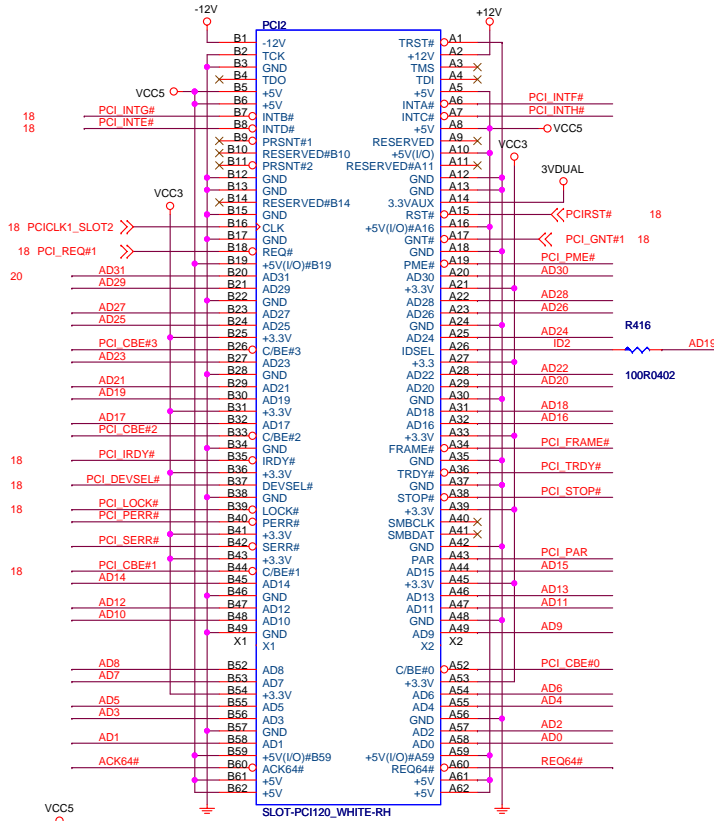
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



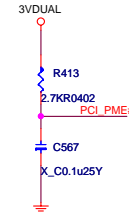
IDSEL = AD18
MASTER = PCI_REQ#0
PCI_GNT#0

ACK#4# R461 8.2KR0402
REQ#4# R420 2.7KR0402

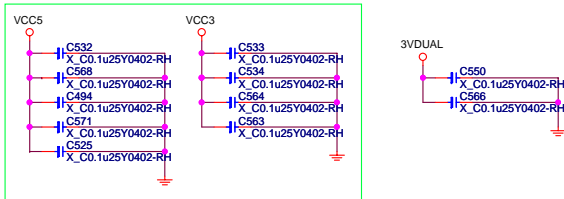
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD19
MASTER = PCI_REQ#1
PCI_GNT#1

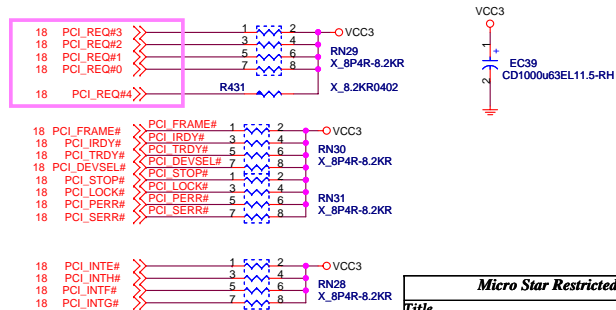


PCI SLOT DECOUPLING CAPACITORS



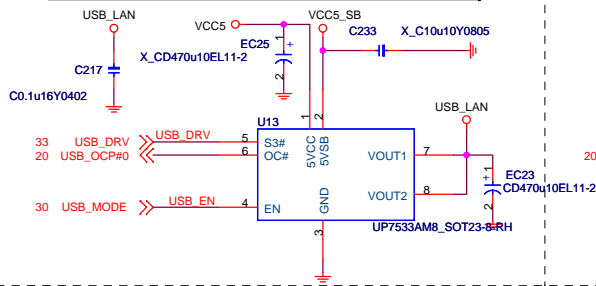
For EMI

PCI PULL-UP / DOWN RESISTORS

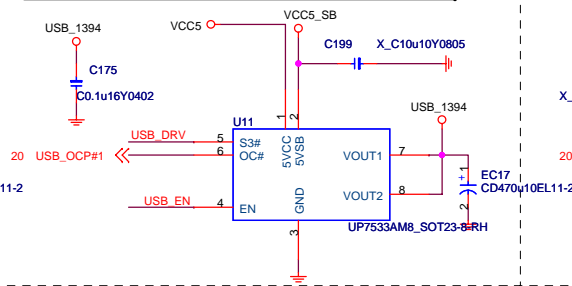


Micro Star Restricted Secret		
Title	PCI Slot 1 2	Rev 0A
Document Number	MS-7501	
MICRO-STAR INT'L CO., LTD. No. 69, L-Hsue St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, December 11, 2007 Sheet 24 of 38

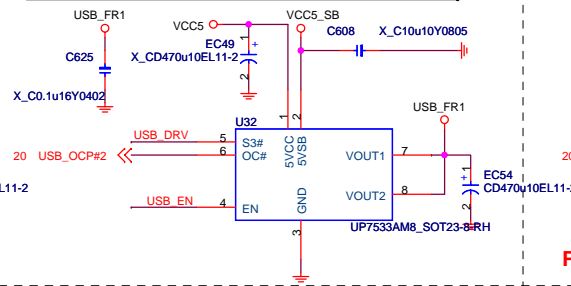
POWER CIRCUIT FOR USB PORT 4,5



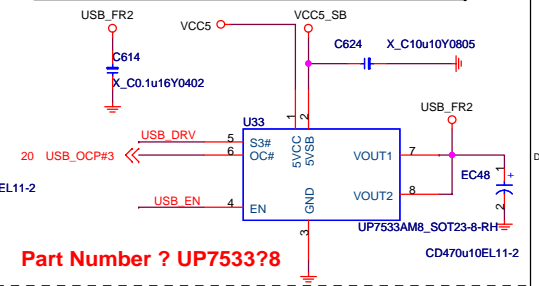
POWER CIRCUIT FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1

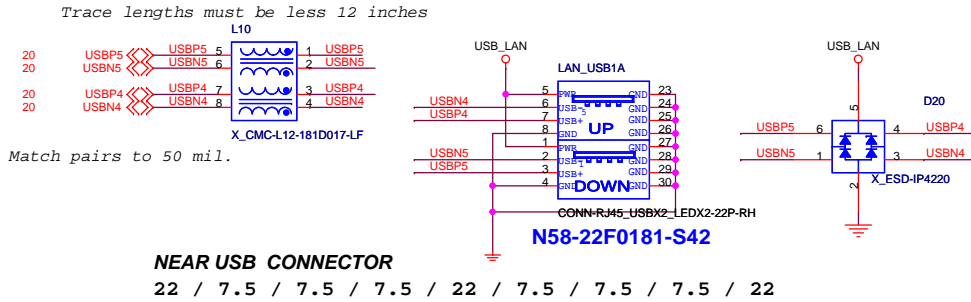


POWER CIRCUIT FOR USB PORT 6,7

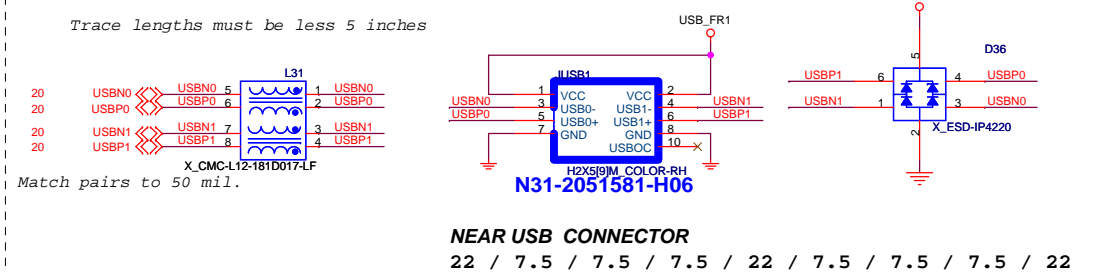


Part Number ? UP7533?8

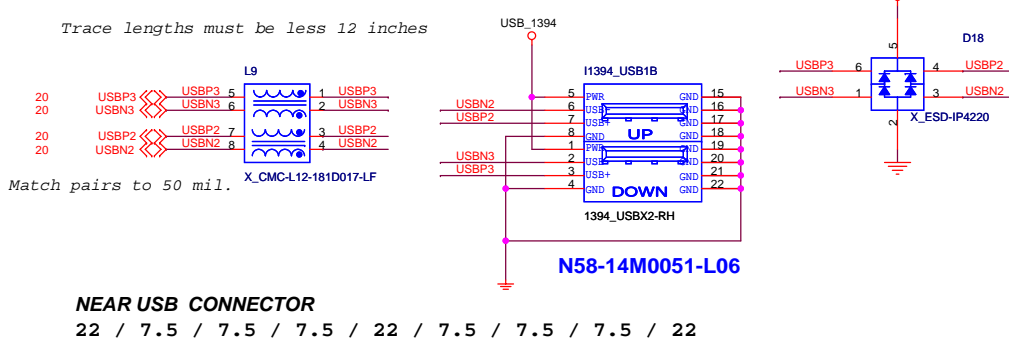
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



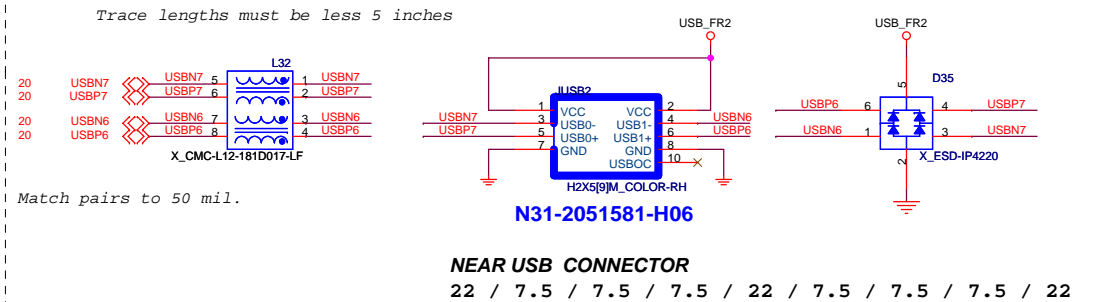
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



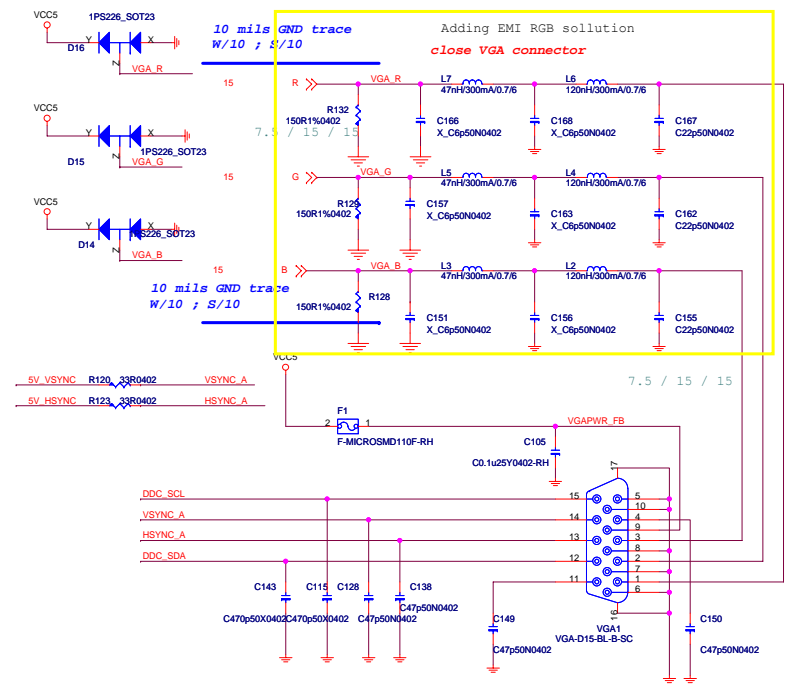
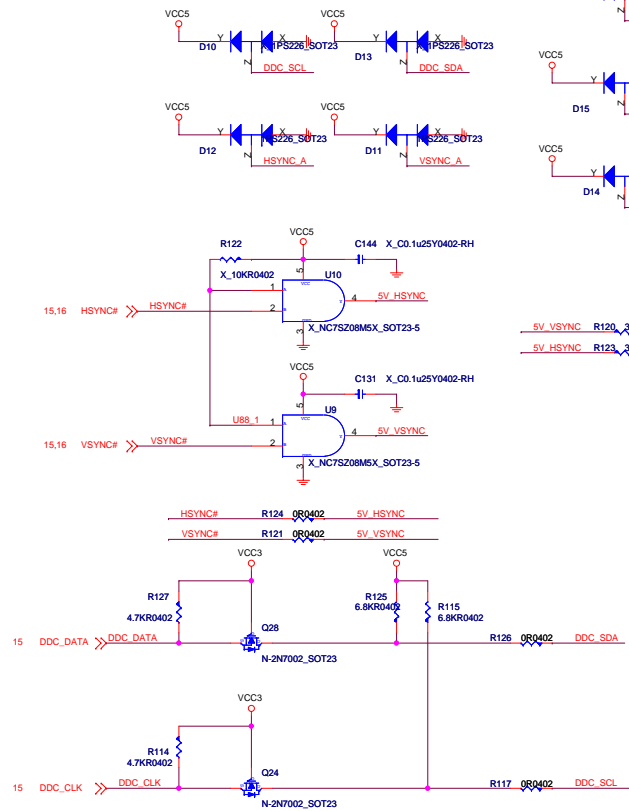
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



MICRO-STAR IN'L CO., LTD.

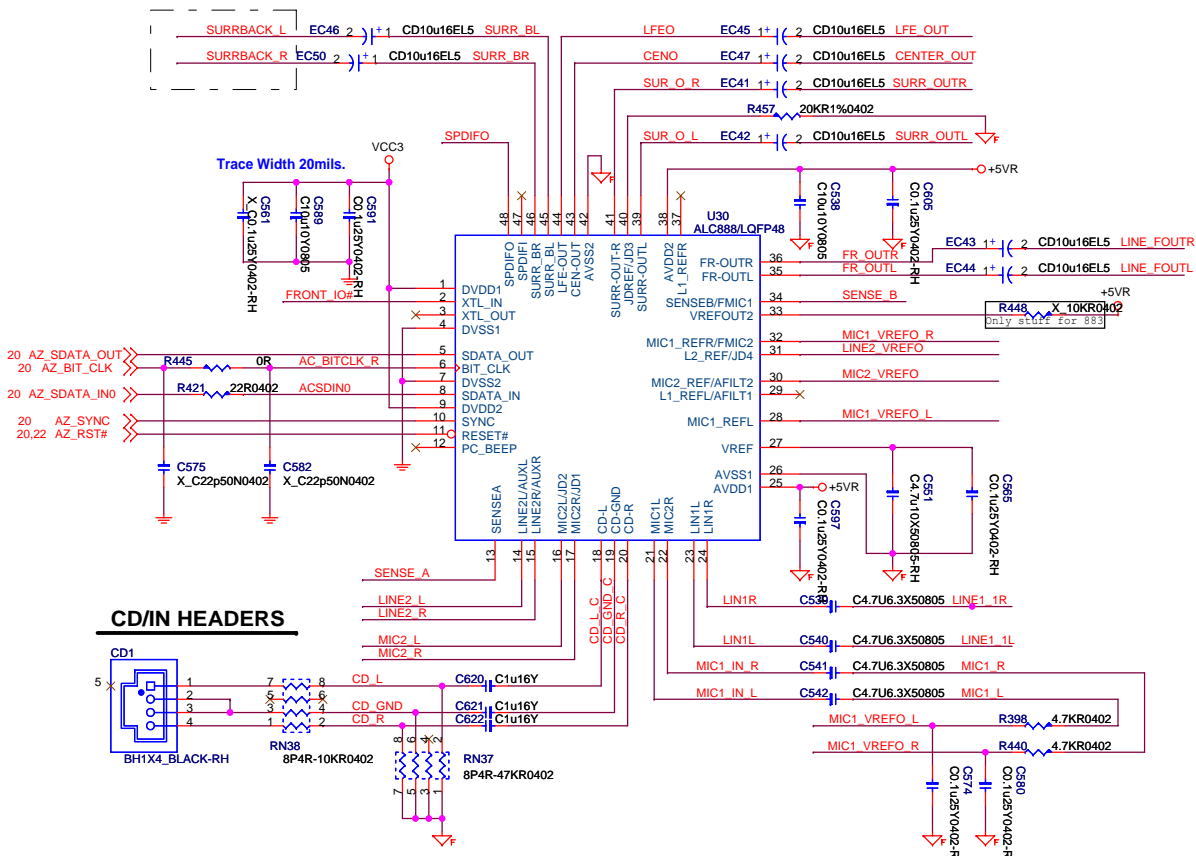
Title			USB Conn.
Size	Document Number	MS-7501	
Date:	Tuesday, December 11, 2007	Sheet	25 of 38

VGA CONN BLOCK



ALC888 CODEC

883 :B09-LC88304-R09
888: B09-LC88804-R09
861D:B09-LC86124-R09

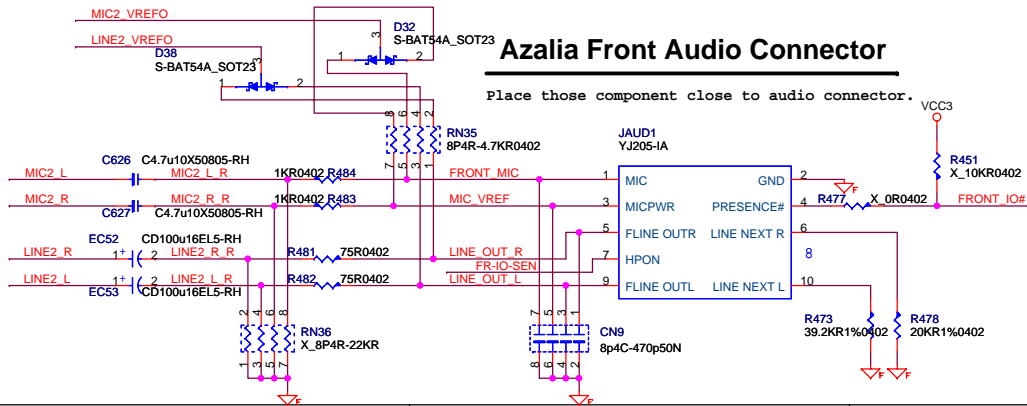


ALC883 JACK DETECT

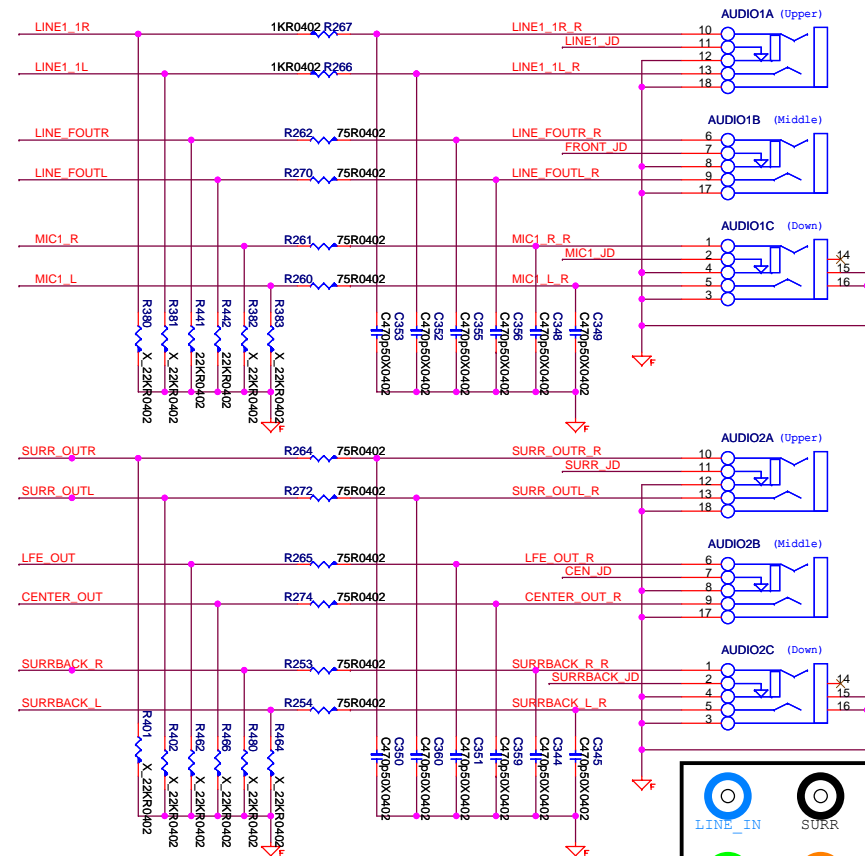


²³ Azalia Front Audio Connector

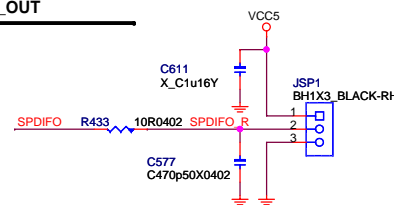
Place those component close to audio connector.



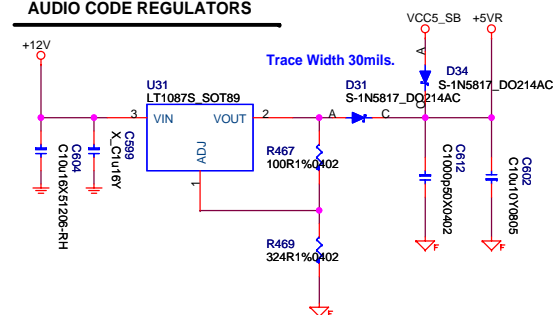
ALC888 JACK



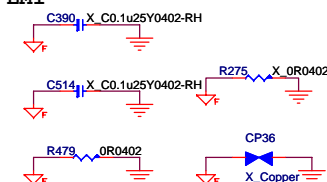
SPDIF_OUT



AUDIO CODE REGULATORS



For EMI



PN:N54-26F0151-S42

MICRO-STAR INT'L CO., LTD.

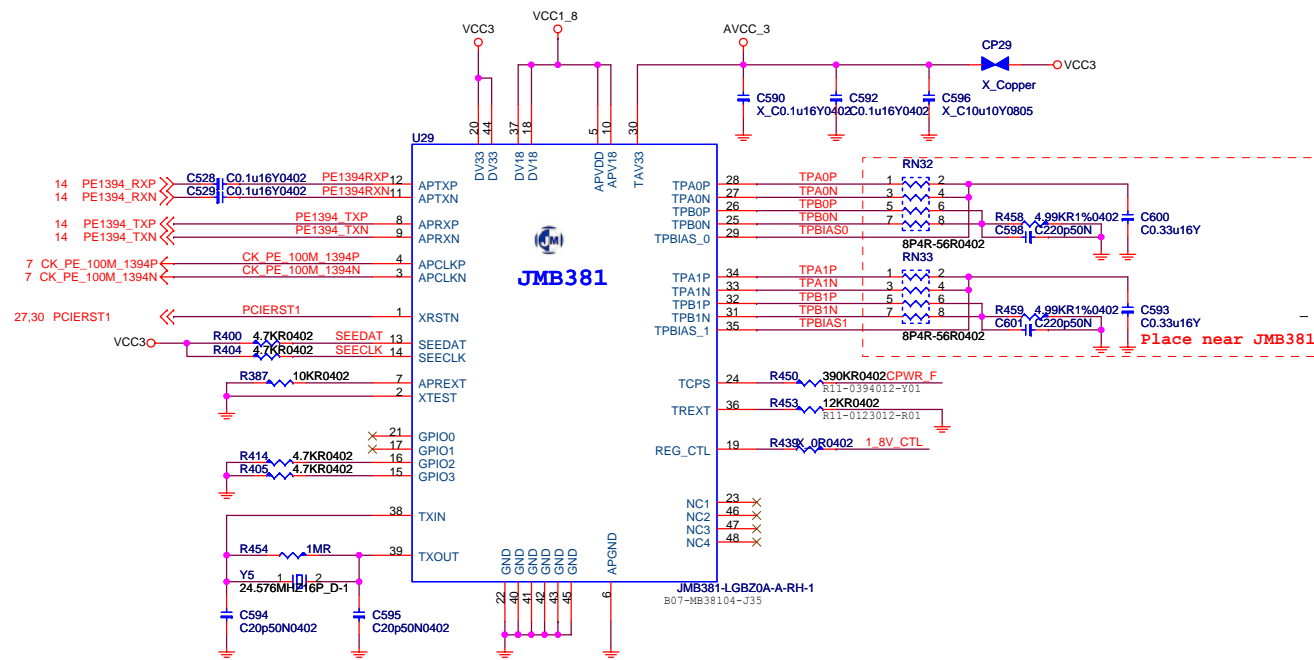
Title	ALC888 CO-LAY ALC883 CODEC
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Size	Document Number
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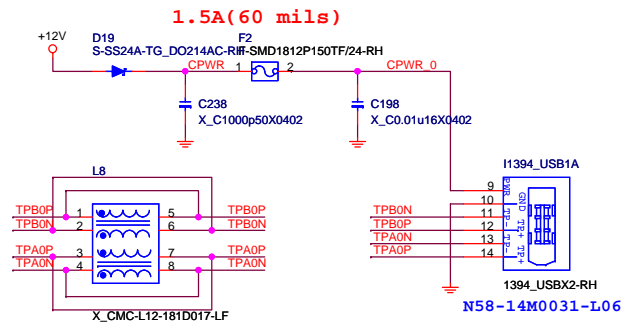
MS-7379

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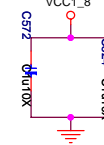
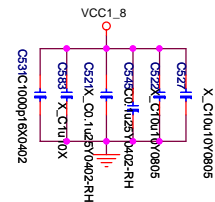
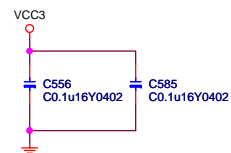
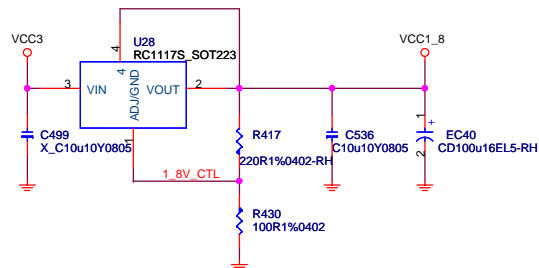
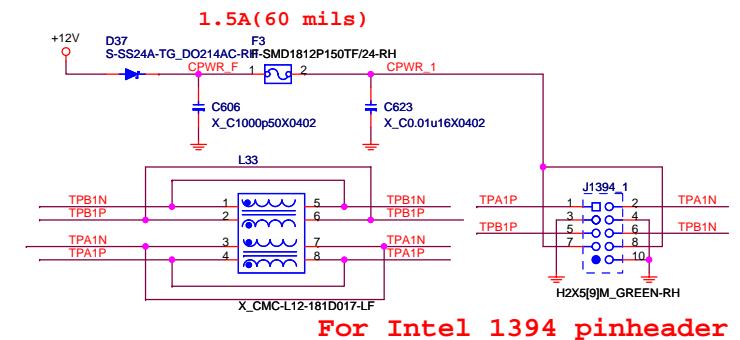
JMICRON JMB381



Rear 1394 port



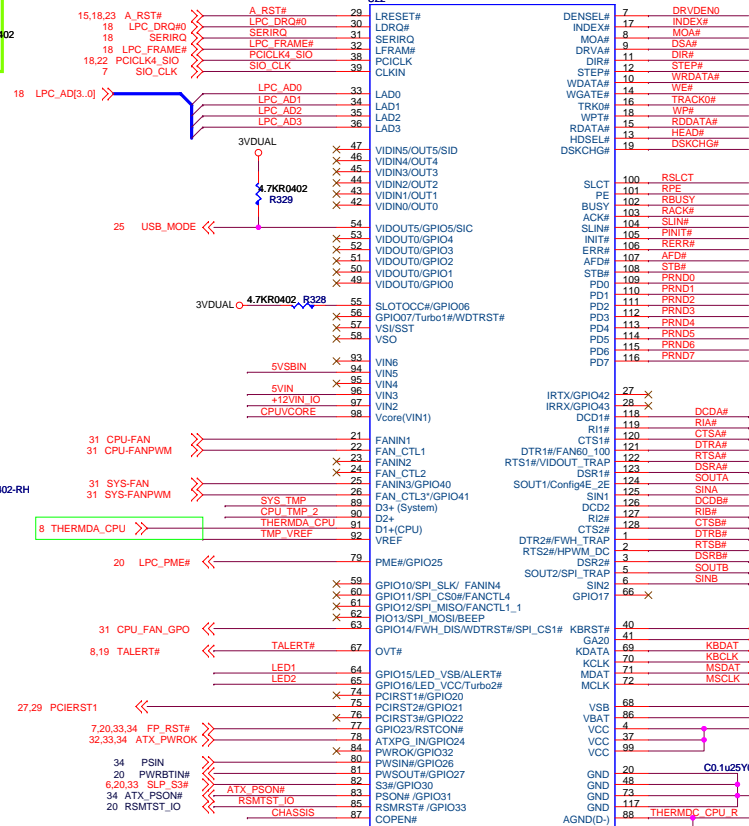
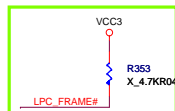
Front 1394 pin header



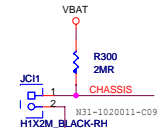
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Date:	Tuesday, December 11, 2007	Sheet 29 of 38	

Super I/O

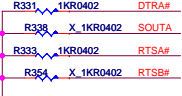
LPC SUPER I/O F71882



Chassis Intrusion

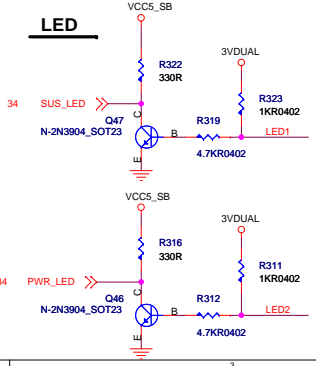


LPC I/O STRAPPING RESISTOR

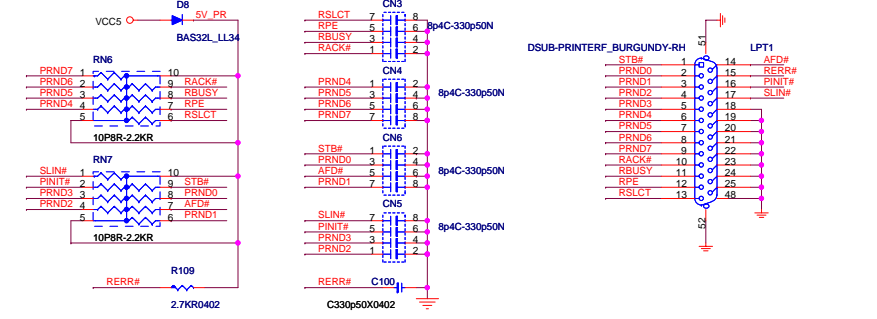


	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT	PIN49-54=GPIO
	PIN42-47=VIDIN	PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

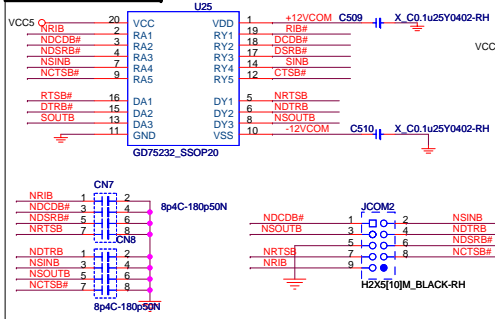
LED



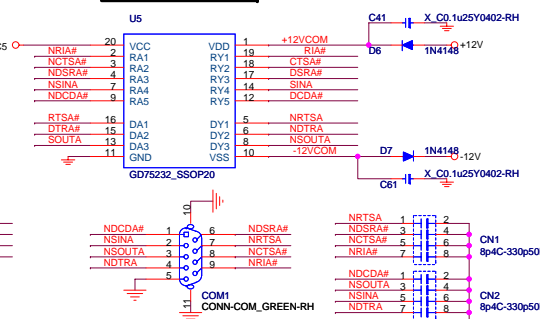
PARALLAL PORT



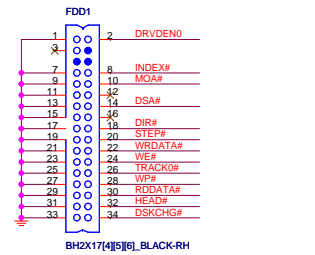
SERIAL PORT 2



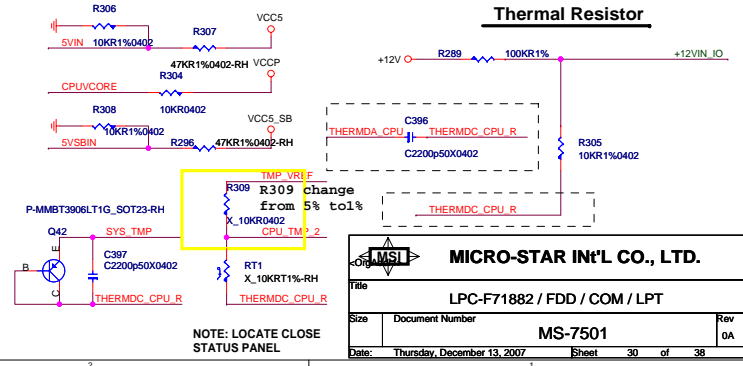
SERIAL PORT 1



FLOPPY CONNECTOR



Thermal Resistor

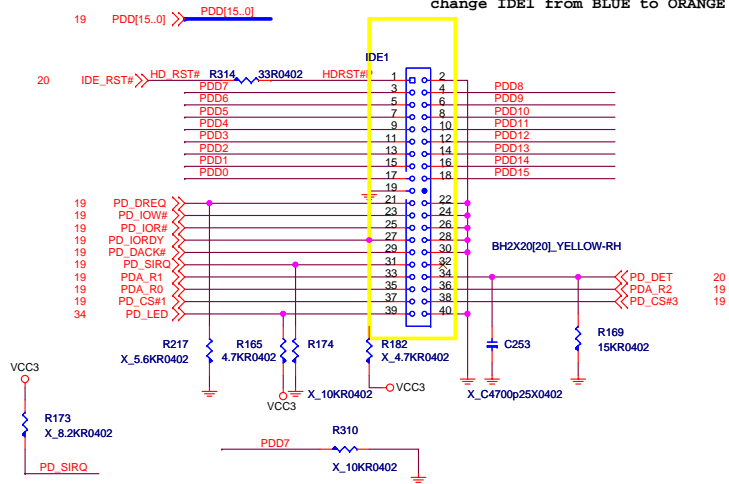


NOTE: LOCATE CLOSE STATUS PANEL

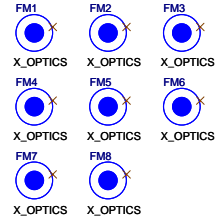
MICRO-STAR INT'L CO., LTD.			
Title: LPC-F71882 / FDD / COM / LPT			
Size	Document Number	Rev	
		0A	
Date: Thursday, December 13, 2007 Sheet 30 of 38			

IDE 1

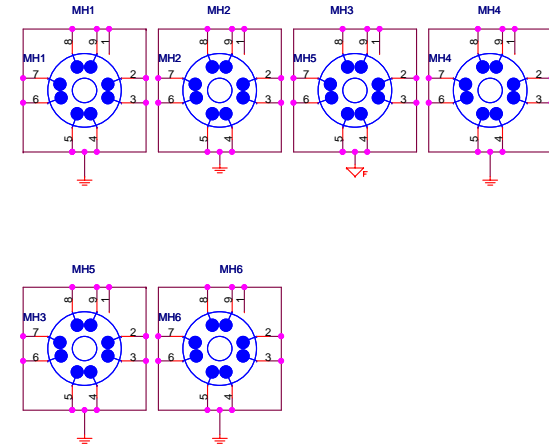
change IDE1 from BLUE to ORANGE



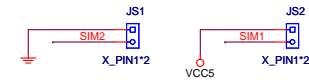
Optics Orientation Holes



Mounting Holes

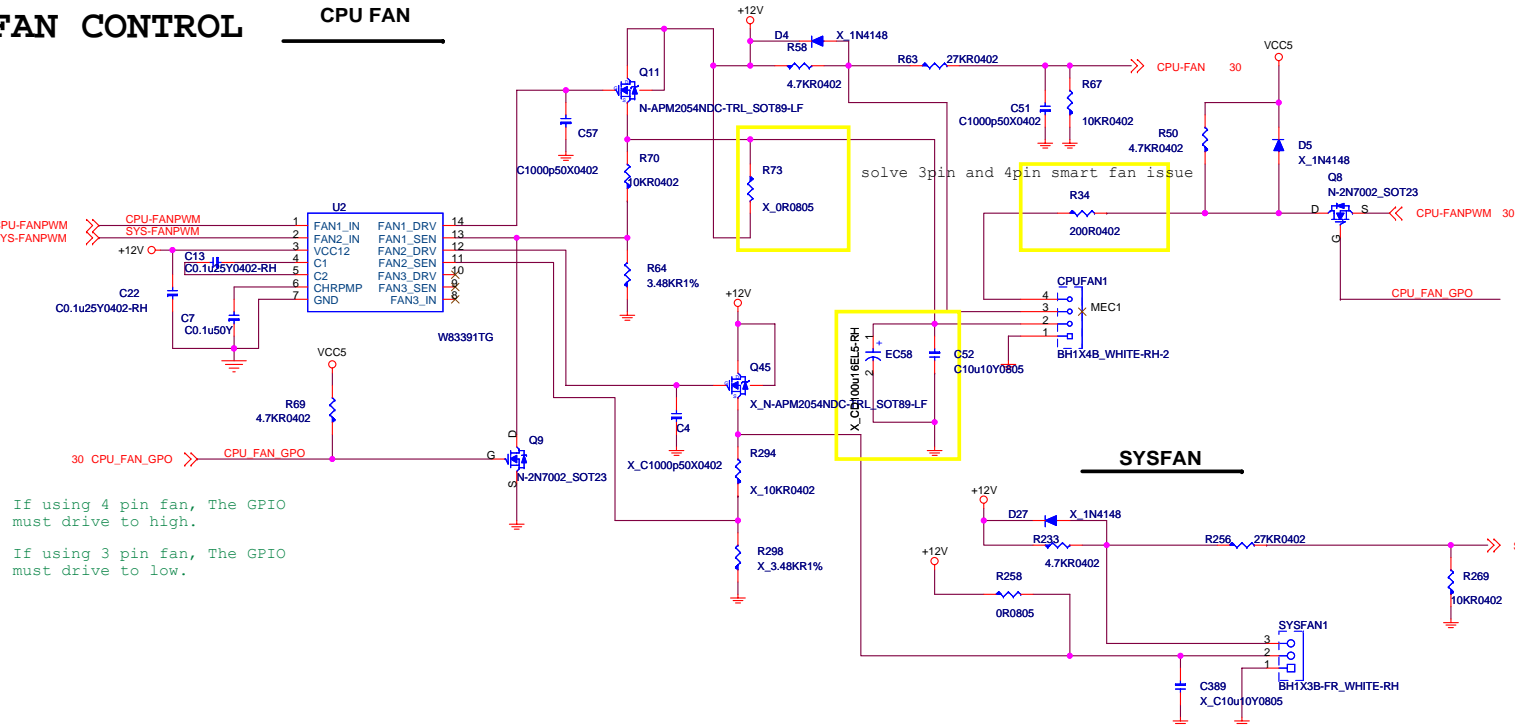


Simulation



FAN CONTROL

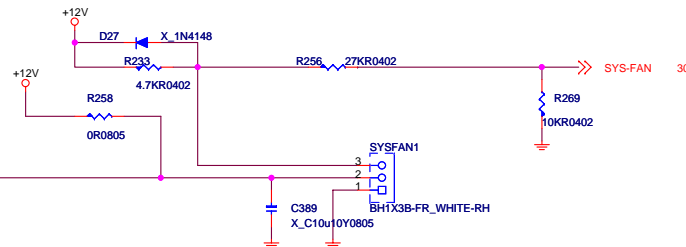
CPU FAN



If using 3 pin fan, The Q40 will turn off to avoid the VCC5(R527) bias to CPU-FANPWM.

solve 3pin and 4pin smart fan issue

SYSFAN



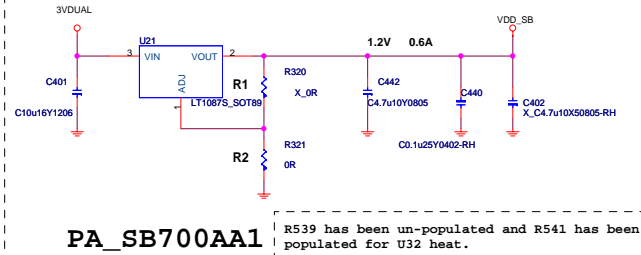
If using 4 pin fan, The GPIO must drive to high.

If using 3 pin fan, The GPIO must drive to low.

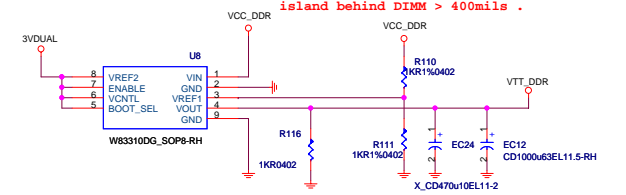
Micro Star Restricted Secret		
Title	IDE Conn / FAN	Rev
Document Number	MS-7501	0A
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, December 12, 2007 Sheet 31 of 38

1.25V reference voltage

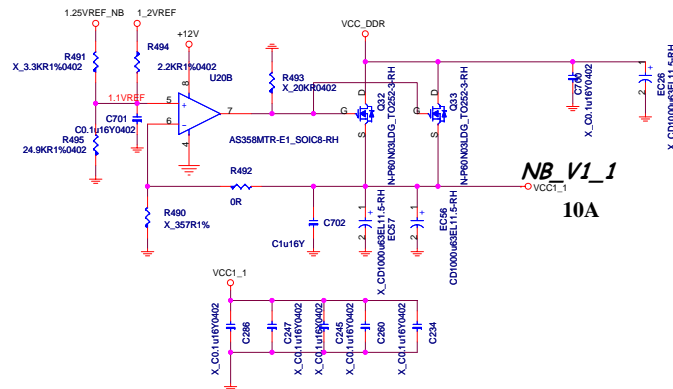
$$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} \times R_2$$



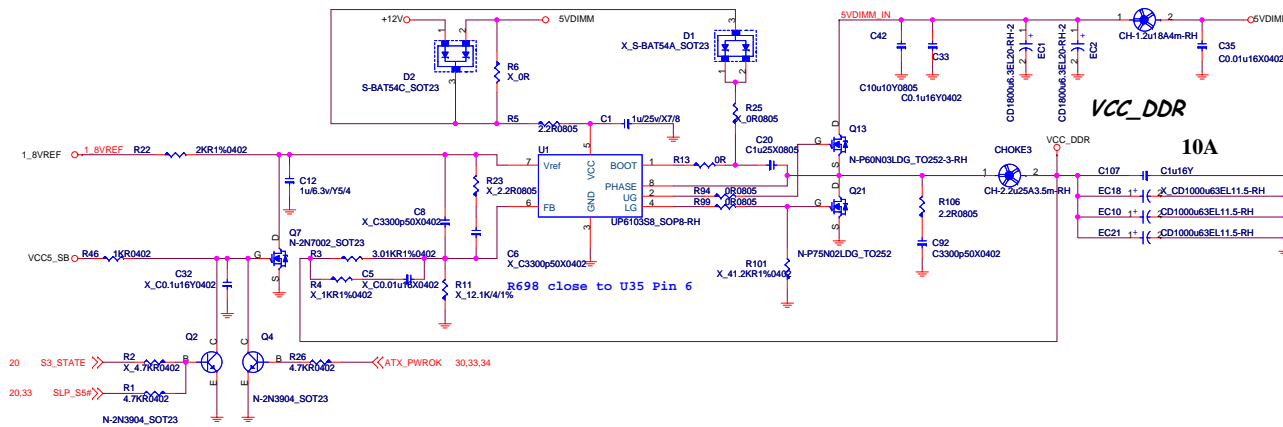
DDR VTT Power



NB 1.1V POWER

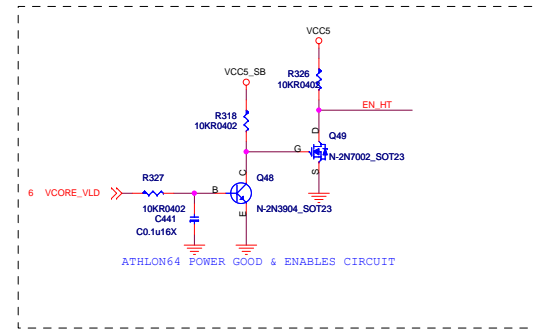
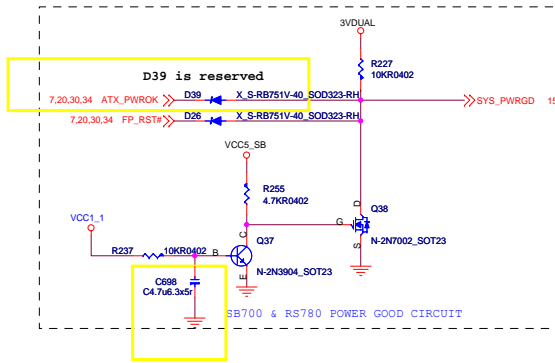
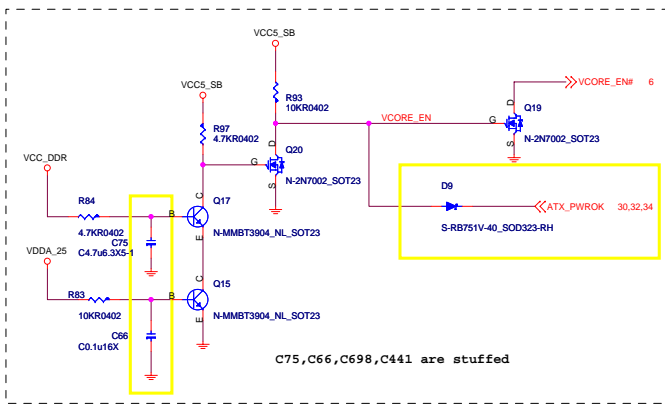


DDR II 1.8V POWER

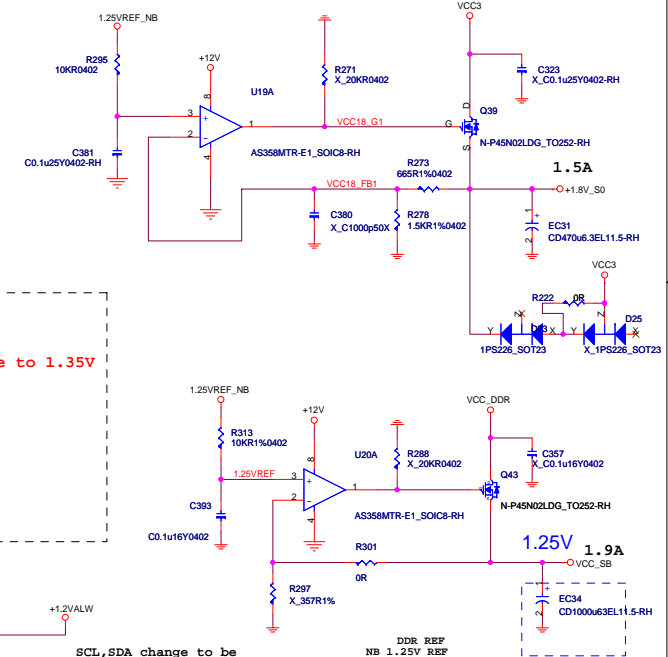
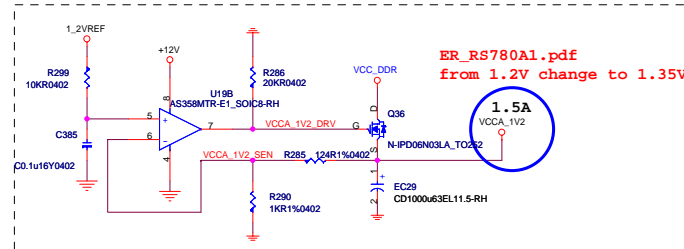
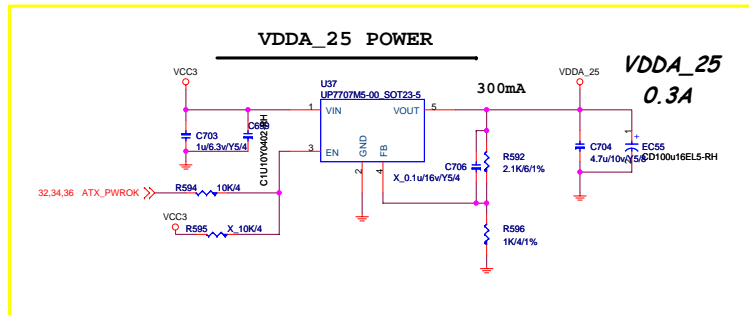


Micro Star Restricted Secret

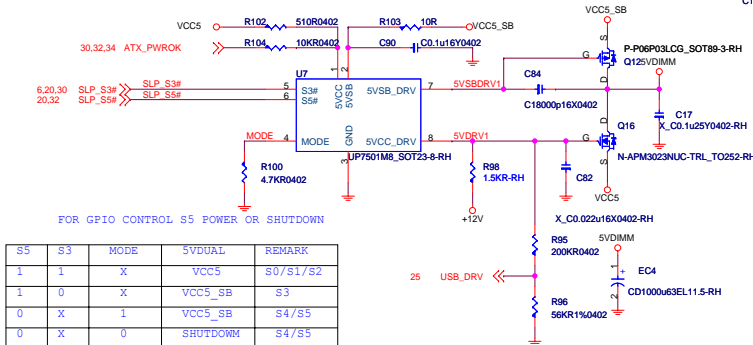
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Document Number		MS-7501
MICRO-STAR INT'L CO., LTD.		Last Revision Date:
No. 69, Li-De St, Jung-Ho City,		Thursday, December 13, 2007
Taipei Hsien, Taiwan		Sheet
http://www.msi.com.tw		32 of 38



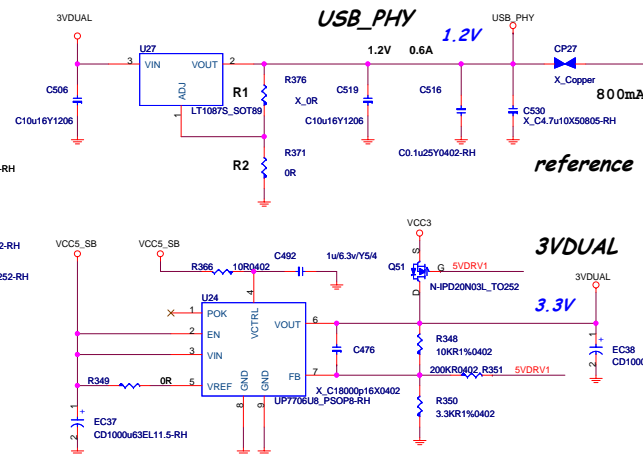
Chage 1087 to 7707 for Power up sequence



5VDIMM FOR DDR



S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWN	S4/S5



SCL, SDA change to be connected to SM BUS0 because that SM BUS1 can not be written

reference Voltage

3VDUAL

3.3V

3.3V

3.3V

3.3V

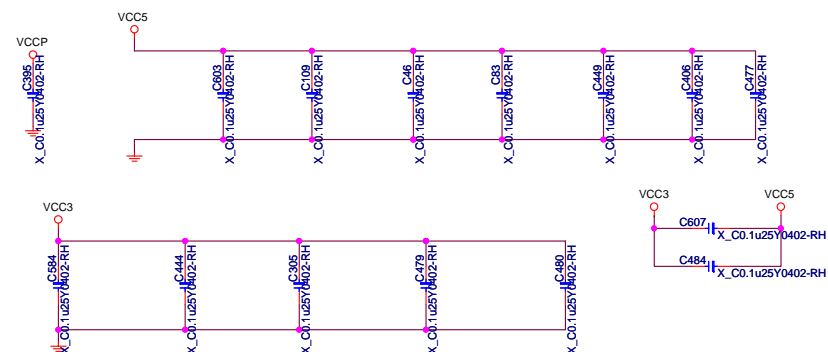
3.3V

3.3V

3.3V

3.3V

Intel Front Panel



Micro Star Restricted Secret		
Title	ATX/Front Panel/KB/EMI	Rev
Document Number	MS-7501	0A
MICRO STAR INT'L CO. LTD. No. 69, L-Jong St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, December 11, 2007 Sheet 34 of 38